Question 1. (4 points)

Explain the terms response time and throughput. For each of the following scenarios, mention which of these two metrics hold more relevance.

Scenario 1: A student needs to compare two smart phones.
Scenario 2: A datacenter manager at Google wants to measure the performance of a server.

Question 2. (3 points)

Give an example of each of the following instruction classes: arithmetic instructions, logical instructions and data transfer instructions in the MIPS assembly language.

Question 3. (3 points)

(I) A processor logically comprises of two major components – datapath and control. Explain what both terms mean. (2 points)
(II) Give two examples of datapath elements: a combinational logic element and a state element. (1 point)

Question 4. (3 points)

Briefly explain each of the following pipeline hazards: structural, data and control hazards.

Question 5. (3 points)

Explain polling and interrupts with regards to I/O devices. What is the advantage of interrupts in comparison to polling?

Question 6. (2 points)

What is a memory cache? What is the difference between a write-through cache and a write-back cache?

Question 7. (2 points)

What is the difference between a TLB miss and a page fault? (with regards to virtual memory).

For the following questions, Q8 to Q13, it is mandatory to write couple of lines of explanation to discuss your approach to solve the problem.

Question 8. (4 points)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. For a given program, the average number of cycles for each instruction class is shown below except for classes B and C in Computer M2. The table also shows how many instructions of a given class are in the program, as a percentage. E.g., if there are 100 instructions in total, there are 60 Class A instructions.

Instruction Class	Computer M1 (Cycles Per Instruction Class)	Computer M2 (Cycles Per Instruction Class)	Percentage of total instruction
A	1	2	60%
B	2	?	30%
C	4	?	10%

The designers of machine M2 aim to have the same average CPI as the one of machine M1. How many cycles should instructions of classes B and C in computer M2 take assuming each instruction takes at least a cycle?

Question 9. (4 points)

Consider the MIPS assembly instructions below. Assume "$a0" contains the address of the first element of a non empty array of 32-bits integers **A** (i.e. "$a0" contains the address of **A**[0]), and that "$a1" contains the number of integers in the array **A**. Write the corresponding C/Java language statement. Write only the arithmetic statement and not the variable declarations (you may introduce other variables in addition to A).

```
      move $t0, $zero
      addi $t1, $zero, 2
loop: sll  $t2, $t0, 2
      add  $t2, $a0, $t2
      sw   $t1, 0($t2)
      addi $t0, $t0, 1
      bne  $t0, $a1, loop
```

Question 10. (2 points)

Convert the numbers 10 and -3 to 16-bit binary numbers (use 2's complement for negative numbers). Perform the addition 10 + (-3) in binary.

Question 11. (4 points)

Consider the datapath shown in Figure 1. Four regions have been marked as A, B, C and D. Answer each one of the following questions:

(i) Region A: what is stored in PC and why is 4 added to its content?

(ii) Region B: give two instructions that result in different values for the control signal ALUSrc. Briefly explain.

(iii) Region C: give an instruction that makes use of the Zero signal. Briefly explain.

(iv) Region D: give two instructions that result in different values for the control signal MemtoReg. Briefly explain.

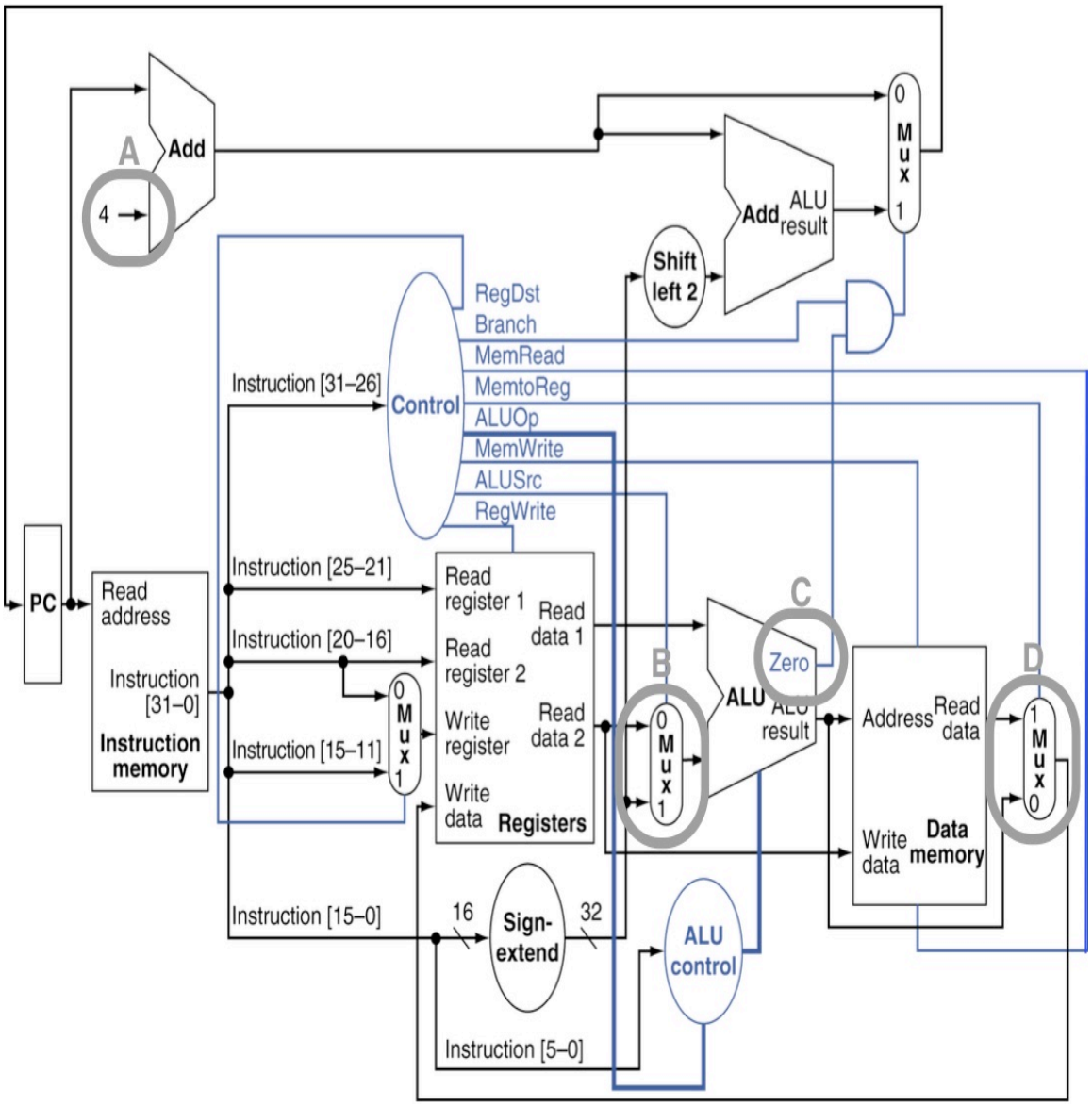


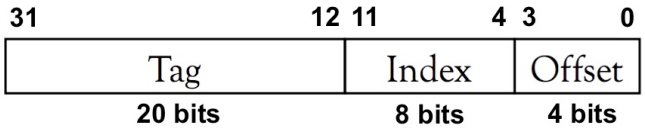
FIGURE 1

Question 12. (3 points)

Draw the pipelined execution corresponding to the code below. Recall that five stages were involved in the lectures: instruction fetch, register read, ALU operation, memory access, and register write. You should not assume forwarding (aka. bypassing) in your answer. Identify possible data-hazards in this code. Can you reschedule the instructions in order to decrease the total number of required cycles while maintaining the same result after execution? What is the number of required cycles before and after rescheduling?

```
lw      $t1, 0($t0)
lw      $t2, 4($t0)
add     $t3, $t1, $t2
lw      $t4, 12($t0)
```

Question 13. (3 points)



Assume a direct mapped cache with 16 bytes per block and 20 bits per tag.

(i) What is the largest number of blocks this cache can contain?
(ii) At which block will a byte at address 4800 be sent?
(iii) What would be the corresponding tag?