Försättsblad till skriftlig tentamen vid Linköpings Universitet

(fylls i av ansvarig)

Datum för tentamen	2014-08-25
Sal	TER1, Terra-salarna i VTI-huset, ingång kortsida
Tid	08-12
Kurskod	TDTS10
Provkod	TEN2
Kursnamn/benämning	Computer Architecture
Institution	IDA
Antal uppgifter som ingår i tentamen	*13*
Antal sidor på tentamen (inkl. försättsbladet)	*7*
Jour/Kursansvarig	*Unmesh Bordoloi*
Telefon under skrivtid	013285628
Kursadministratör (namn + tfnnr + mailadress)	*Helene Meisinger 281868, helene.meisinger@liu.se*
Tillåtna hjälpmedel	
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

Linköping University
25th August 2014

TDTS10 Exam
Computer Architecture

Jour : Unmesh Bordoloi (46 13 28 56 28)

- **Admitted materials**
  - Dictionary between your native language and English

- **General instructions**
  - You may answer in Swedish or in English.
  - Write clearly, unreadable text will be ignored.
  - The exam is for 40 points. At least **13 points** are necessary for passing this course.

Question 1. (4 points)

Explain the terms response time and throughput. For each of the following scenarios, mention which of these two metrics hold more relevance.

Scenario 1: A student needs to compare two different desktop computers.
Scenario 2: A datacenter manager at Facebook wants to measure the performance of a server.

Question 2. (3 points)

Give an example of each of the following instruction classes: arithmetic instructions, logical instructions and data transfer instructions in the MIPS assembly language.

Question 3. (3 points)

(I) A processor logically comprises of two major components – datapath and control. Explain what both terms mean. (2 points)
(II) What is the main difference between a combinational logic and a state element in a datapath? (1 point)

Question 4. (3 points)

The following table incorrectly maps the 3 types of pipeline hazards with their solutions. Write down the correct table.

Type of hazard	Solution
Structural hazard	Brach prediction
Data hazard	Separation of instruction and data memory
Control hazard	Forwarding/Bypassing

Question 5. (3 points)

With regards to I/O devices what is the difference between polling and interrupts? Which one of them may lead to wastage of CPU time and why?

Question 6. (2 points)

What is meant by a bus in a computer system? What is the difference between a synchronous and an asynchronous bus?

Question 7. (2 points)

Who gets the control when there is a page-fault (with regards to virtual memory – is it the operating system or is it the hardware? Why?

For the following questions, Q8 to Q13, it is mandatory to write couple of lines of explanation to discuss your approach to solve the problem.

Question 8. (4 points)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. For a given program, the average number of cycles for each instruction class is shown below except for the class A in Computer M2. The table also shows how many instructions of a given class are in the program, as a percentage. E.g., if there are 100 instructions in total, there are 60 Class A instructions.

Instruction Class	Computer M1 (Cycles Per Instruction Class)	Computer M2 (Cycles Per Instruction Class)	Percentage of total instruction
A	1	?	60%
B	2	3	30%
C	4	5	10%

Given that the machine M2 has average CPI that is twice that of machine M1, find the number of cycles for the class A in computer M2.

Question 9. (4 points)

Given the MIPS assembly language instructions in the following two cases, write the corresponding C/Java language statement for both of them. Write only the arithmetic statement and not the variable declarations.

For both cases, also give the end value of the register **f** if **f, g, h, i** have the values 1, 2, 3, and 4. Remember that MIPS instructions are of the following format : InstructionName R1, R2, R3 where R3 and R2 are source registers and R1 is a destination register.

(a) addi f, f, 4

(b) add f, g, h
add f, i, f

Question 10. (2 points)

Perform the following operation by converting the numbers to 16 – bit binary numbers. Use 2's complement for subtraction.

8 - 12

Question 11. (4 points)

Consider the datapath shown in Figure 1. Assume that the processor has only ALU instructions (ADD, AND, etc.). Also, assume that there is NO pipelining. Consider that the logic blocks have the latencies as shown in Table 1. Other units have negligible latencies.

(i) Which units in the data-path are used? (2 points)
(ii) What would be the clock cycle-time for this datapath? (2 points)

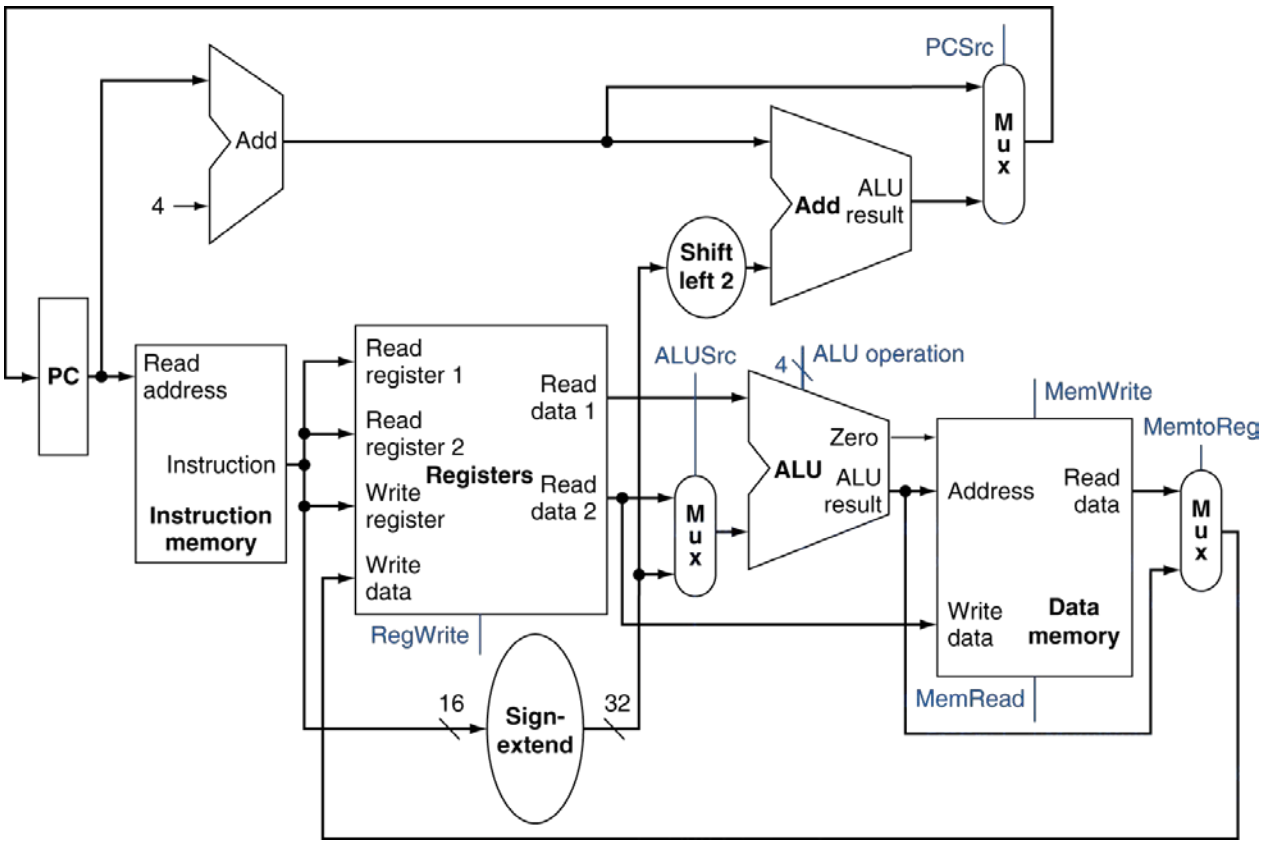

FIGURE 1

I-Mem	ADD	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2
200 ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

TABLE 1

Question 12. (3 points)

In the following MIPS instruction sequence, there are 3 data dependencies that can potentially be data hazards. Identify the three dependencies (the variables and the instruction labels). It is not required to show the pipelined execution.

```
I1:   ADD  R1,  R2,  R1
I2:   LW   R2,  0(R1)
I3:    LW  R1,  4(R1)
I4:   OR   R3,  R1,  R2
```

Question 13. (3 points)

For the following code, identify the variables that exhibit temporal locality and the variables that exhibit spatial locality. The variables are I, J, A.

```
for (I = 0; I < 8; I++)
        for (J = 0; J < 8000; J++)
                A [ I ] [ J ] = 5 + A [ J ] [ I ];
```
