Linköping University
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TDTS10 Exam
Computer Architecture

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- **Admitted materials**
  - Dictionary between your native language and English

- **General instructions**
  - You may answer in Swedish or in English.
  - Write clearly, unreadable text will be ignored.
  - The exam is for 40 points. At least **13 points** are necessary for passing this course.

Question 1. (3 points)

Computer A has an overall CPI of 1.3 and can be run at a clock rate of 600MHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 750 Mhz. We have a particular program we wish to run. When compiled for computer A, this program has exactly 100,000 instructions. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program?

Question 2. (3 points)

Prior to the early 1980s, machines were built with more and more complex instruction set. Howevr RISC machines are more popular now. Why has there been a move to RISC machines away from complex instruction machines?

Question 3. (4 points)

Write the following sequence of code into MIPS assembler:

x = x + y + z - q;Assume that x, y, z, q are stored in registers $s1-$s4.

Question 4. (3 points)

Perform the following operation by converting the operands to 2's complement binary numbers and then doing the addition or subtraction shown. Please show all work in binary, operating on 16-bit numbers.

13 – 2

Question 5. (4 points)

Consider the datapath shown in Figure 1. Assume that the processor has only one type of instruction: the 'conditional' jump instruction that executes a jump relative to the address in PC (Program Counter) after comparing register values. Also, assume that there is NO pipelining. Consider that the logic blocks have the latencies as shown in Table 1. Other units have negligible latencies.

1. What units of the datapath will used in this processor? Explain the reason.
2. What would be the cycle-time for this datapath? Show your working.

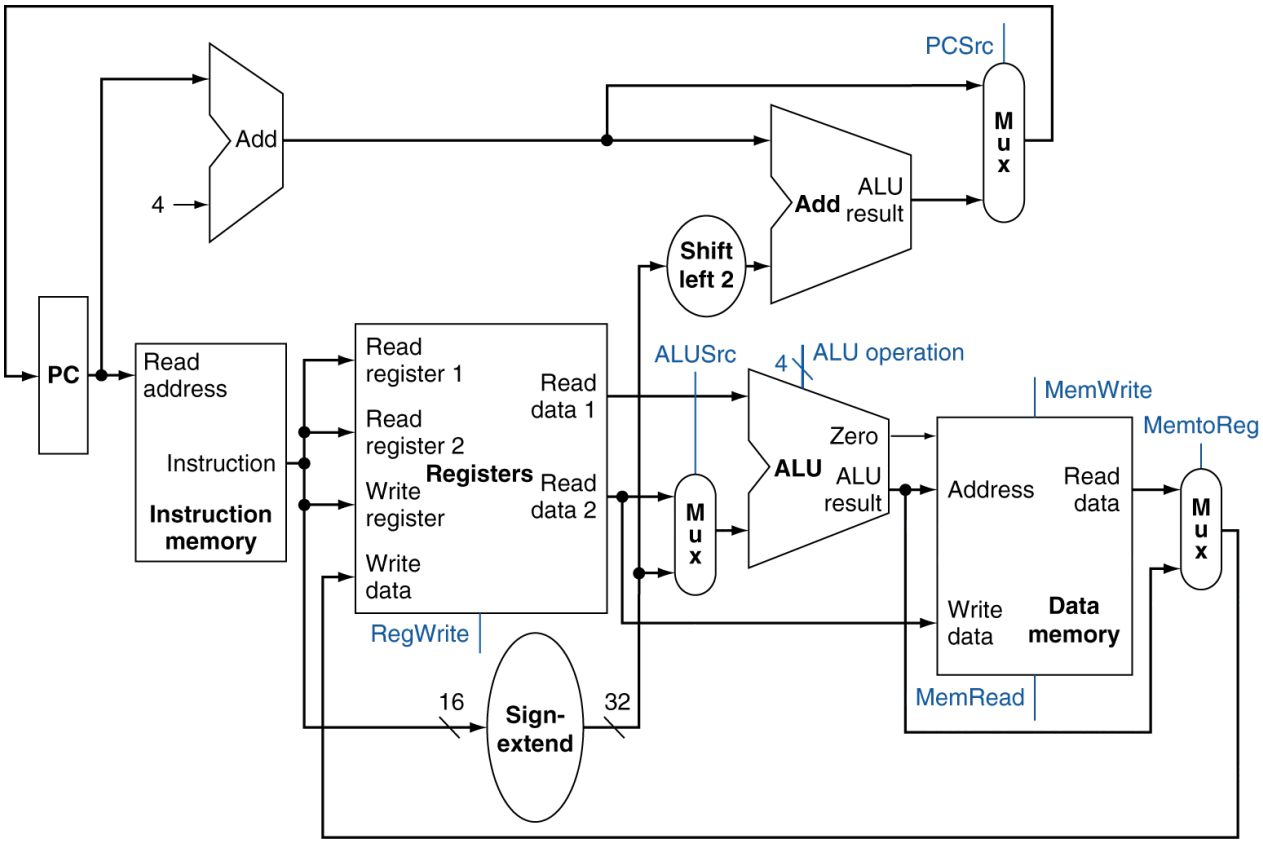

FIGURE 1

I-Mem	ADD	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2
200 ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

TABLE 1

Question 6.

In this question, assume that all branches are perfectly predicted (this eliminates all control hazards). To resolve other hazards, pipeline must be stalled. Assume that we have only one memory (for both instructions and data). Also assume that there is no forwarding.

(i) Show the pipelined execution for each instruction. **(2 points)**

(ii) Identify the hazards that occurred and show where. **(2 point)**

(iii) How many cycles did the pipeline stall? **(1 point)**

```
            SW   R2,  0(R3)
            OR   R1,  R2,  R3
            BEQ  R2,  R0,  Label  (Assume R2== R0)
            OR   R2,  R2,  R0
Label :     ADD       R1,  R4,  R3
            AND  R3,  R2,  R3
```

Question 7. (3 points)

Design a 8-way set associative cache that has 16 blocks and 32 bytes per block. Assume a 32 bit address. Calculate the following:

(a) How many bits are used for the byte offset?

(b) How many bits are used for the set (index) field?

(c) How many bits are used for the tag?

Question 8. (6 points)

Answer each of the following questions.

(a) What is memory mapped I/O?

(b) Why is DMA an improvement over CPU programmed I/O?

(c) When would DMA transfer be a poor choice?

Question 9. (2 points)

Mention advantage and disadvantage for using a single bus as a shared communication link between memory, processor and I/O devices.

Question 10. (4 points)

A processor logically comprises of two major components – datapath and control. Explain in detail with examples what both terms mean.

Question 11. (3 points)

The following table incorrectly maps the 3 types of pipeline hazards with their solutions. Write down the correct table.

Type of hazard	Solution
Structural hazard	Brach prediction
Data hazard	Separation of instruction and data memory
Control hazard	Forwarding/Bypassing