Försättsblad till skriftlig tentamen vid Linköpings Universitet

(fylls i av ansvarig)

Datum för tentamen	2014-01-15
Sal	TER2
Tid	(8-10)
Kurskod	TDTS10
Provkod	TEN2
Kursnamn/benämning	Computer Architecture
Institution	IDA
Antal uppgifter som ingår i tentamen	*10 questions*
Antal sidor på tentamen (inkl. försättsbladet)	*7 pages excluding försättsbladet*
Jour/Kursansvarig	*Unmesh Bordoloi*
Telefon under skrivtid	*0766348968*
Besöker salen ca kl.	
Kursadministratör (namn + tfnnr + mailadress)	*Helene Meisinger 281868, helene.meisinger@liu.se*
Tillåtna hjälpmedel	*Language dictionary*
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

Linköping University
15th January 2014

TDTS10 Exam
Computer Architecture

Jour : Unmesh Bordoloi (07 66 34 89 68)

- **Admitted materials**
  - Dictionary between your native language and English

- **General instructions**
  - You may answer in Swedish or in English.
  - Write clearly, unreadable text will be ignored.
  - The exam is for 40 points. At least 10 points are necessary for passing this course.

Question 1. (6 points)

You are a technical consultant at an IT company that has been hired by our university. Your company will provide infrastructure for a new kind of classroom technology.

First, it will provide computers to the students. These simple computers will be used by students to respond to in-lecture quizzes (only multiple-choice questions), check their grades even if they are travelling, or post small notes to classroom forums and share news feeds about class events in very fast manner. These computers must be portable so that students may easily carry them around and will not support any other functionality apart from those mentioned above. They cannot be easily connected to an electrical source for power because there are many students in each lecture room, and hence batteries drive them.

Second, all the data collected during class polls, students' grades uploaded by teachers and any other teaching related data will be stored away in a powerful computer given by your company to our university. Thus, this computer will be a centralized repository of all the information that students and teachers are always using. This central computer services all requests made from the small computers of the students.

Finally, teachers also need to access the results of classroom quizzes and polls *on-line* when delivering the lectures. Hence, the company will also provide a computer to each room near the front of the lecture hall. This computer need not be very small. However, it must have enough computational capacity to process the results of the responses of students to classroom quizzes and plot graphs and trends. It must be powerful enough to support word & power-point like tools to assist the teachers. It must also support code development so that the teacher can use it for live demonstrations in lectures. Eventually, however all data will be uploaded to the central computer by this computer in the classroom.

Now, recall the three classes of computers from our lecture notes. As a consultant, which class of computer would you recommend to your company for each of the three scenarios described above? Explain the reason for each of your choice.

What performance criteria (throughput/response-time) would you use for each scenario?

Question 2. (2 points)

Assume that the program below is stored in the RAM memory.

Address	Instruction/Data
0	LOAD R2, 10(R3)
1	LOAD R1, 20(R3)
2	ADD R1, 50 (R2)
3	JUMP 5
4	ADD R1, R2, R3
5	MUL R1, R2, R6
6	HLT

Is it possible, given the program above, to determine if it is a RISC or CISC processor? Motivate your answer.

Question 3.

(a) What is the corresponding binary number of the decimal number 32930?
(2 points)

(b) How many bits (binary digits) were required to write the binary number? Let us say this number of bits is *n*.
(1 point)

(c) Using this number *n* that you found, now answer the following question.

Assume that you, as a computer architect, are allowed to use *n* bits for instruction encoding for a designing a processor. Imagine a special processor, where there are only 8 registers (0 to 7) and there are only 16 instructions. Assume that you do not need to encode anything else apart from the register operands and the instructions.

How many register operands can you specify in a single instruction?

Lets us say this number you found is x. Do you think it makes sense (i.e., is practical) to design a processor where you can specify x register operands?
(3 points)

Question 4. (4 points)

Write the C or Java statement for the following MIPS assembly language.

Assume f is stored in $s0 and g in $s1. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. A and B are arrays of 'words', where each word is 32 bits.

```
sll   $t0,  $s0,  2     Hint: What arithmetic does shift left accomplish?
add   $t0,  $s6,  $t0   Hint: What address does $t0 point to now?
sll   $t1,  $s1,  2
add   $t1,  $s7,  $t1
lw    $s0,  0($t0)
addi  $t2,  $t0,  4
lw    $t0,  0($t2)
add   $t0,  $t0,  $s0
sw    $t0,  0($t1)
```

Question 5.

(I) What is the principle of locality? What are the two types of locality that are typically seen? **(2 points)**

(II) Give an example of a program snippet for each type. **(2 points)**

Question 6. (4 points)

Consider the datapath shown in Figure 1. Assume that the processor has only one type of instruction: the R-type instruction 'Add'. Also, assume that there is NO pipelining. Consider that the logic blocks have the latencies as shown in Table 1. Other units have negligible latencies.

1. What units of the datapath will used in this processor? Explain the reason.
2. What would be the cycle-time for this datapath? Show your working.

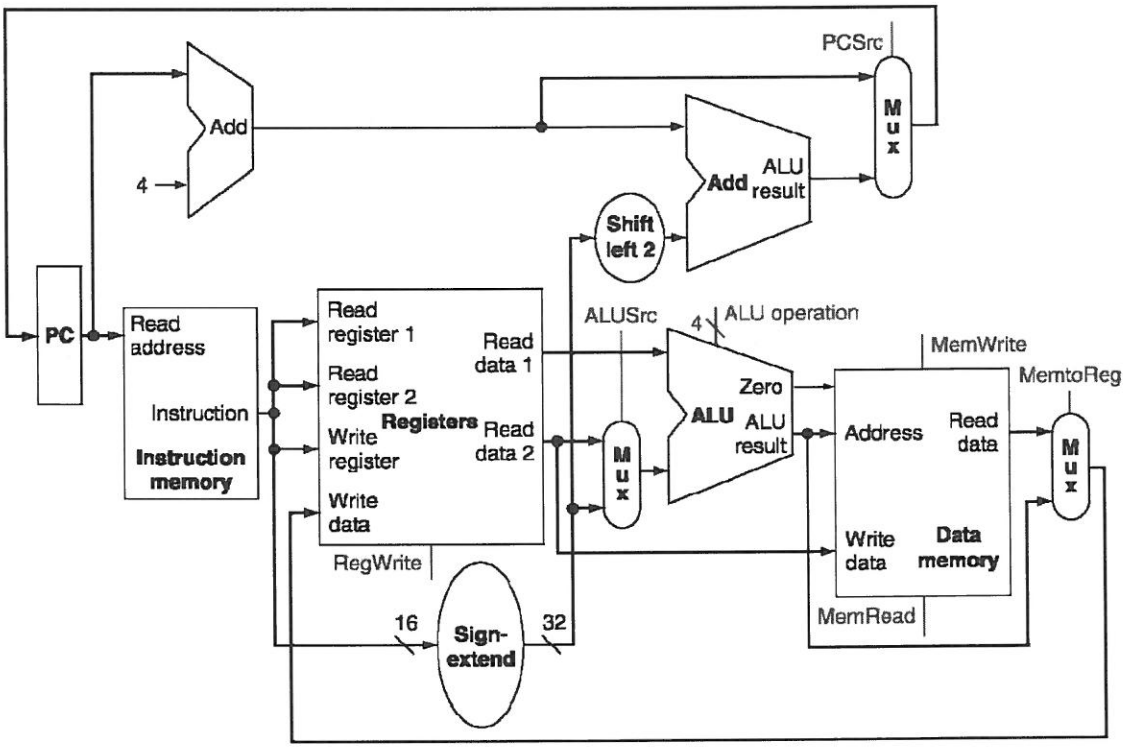

FIGURE 1

I-Mem	ADD	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2
200 ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

TABLE 1

Question 7.

In this question, assume that all branches are perfectly predicted (this eliminates all control hazards). To resolve other hazards, pipeline must be stalled. Assume that we have only one memory (for both instructions and data). Also assume that there is no forwarding.

(i) Show the pipelined execution for each instruction. **(2 points)**

(ii) Identify the hazards that occurred and show where. **(2 point)**

(iii) How many cycles did the pipeline stall? **(1 point)**

```
        SW    R2,   0(R3)
        OR    R1,   R2,   R3
        BEQ   R2,   R0,   Label  (Assume R2== R0)
        OR    R2,   R2,   R0
Label : ADD   R1,   R4,   R3
        AND   R3,   R2,   R3
```

Question 8. (3 points)

Design a 128KB direct-mapped data cache that uses a 32-bit address and 16 bytes per block. Calculate the following:

(a) How many bits are used for the byte offset?

(b) How many bits are used for the set (index) field?

(c) How many bits are used for the tag?

Question 9. (3 points)

Suppose we have two different I/O systems A and B. A has data transfer rate: 5KB/s and has access delay: 5 sec. While B has data transfer rate: 3 KB/s and has access delay: 4 sec. Now, if we have a 3MB I/O request, taking performance into consideration, which I/O system will you use? What about for a 3KB request? Access delay in an I/O system means the delay required in initializing the I/O system. During the initialization, no data is transferred. After the initialization, the data is transferred with the given data transfer rate.

Question 10. (3 points)

With regards to I/O devices what is the difference between polling and interrupts? Which one of them may lead to wastage of CPU time and why?
