Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	18 December 2012
Sal	T1 and KÅRA
Tid	14 to 18
Kurskod	TDTS10
Provkod	TEN2
Kursnamn/benämning	Computer Architecture
Institution	*IDA*
Antal uppgifter som ingår i tentamen	14 questions
Antal sidor på tentamen (inkl. försättsbladet)	5 pages of questions plus one for this page
Jour/Kursansvarig	Unmesh Bordoloi
Telefon under skrivtid	0766348968
Besöker salen ca kl.	About 1 hour after exam
Kursadministratör (namn + tfnnr + mailadress)	Madeleine Häger Dahlqvist, madeleine.hager.dahlqvist@liu.se
Tillåtna hjälpmedel	Dictionary between English and native language of the student
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

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Linköping University
18th December 2012

TDTS10 Exam
Computer Architecture

Jour : Unmesh Bordoloi (07 66 34 89 68)

- **Admitted materials**
  - Dictionary between your native language and English

- **General instructions**
  - You may answer in Swedish or in English.
  - Write clearly, unreadable text will be ignored.
  - The exam is for 40 points. At least 10 points are necessary for passing this course.
  - If a question is clearly divided into sub-parts, the points for sub-parts are also shown.

Question 1. (2 points)

Give two differences between RISC and CISC processors.

Question 2. (2 points)

What is the advantage of separate data and instruction caches when it comes to performance in a pipelined architecture? Give an example to support your answer.

Question 3. (3 points)

(I) A processor logically comprises of two major components – datapath and control. Explain what both terms mean. (2 points)
(II) What is the main difference between a combinational logic and a state element in a datapath? (1 point)

Question 4. (3 points)

(I) With regards to I/O devices what is the difference between polling and interrupts? (1 point)
(II) Which one of them may lead to wastage of CPU time and why? (2 points)

Question 5. (5 points)

(I) What is the principle of locality? (1 point)
(II) What are the two types of locality that are typically seen? (2 points)
(III) Give an example of program characteristics for each type. (2 points)

Question 6. (2 points)

What is meant by a bus in a computer system? What is the difference between a synchronous and an asynchronous bus?

Question 7. (3 points)

(i) Who gets the control when there is a page-fault (with regards to virtual memory – is it the operating system or is it the hardware? Why? (2 points)
(ii) Why is this different in the scenario of a cache miss? (1 point)

For the following questions, Q8 to Q14, it is mandatory to write couple of lines of explanation to discuss your approach to solve the problem.

Question 8. (4 points)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. For a given program, the average number of cycles for each instruction class is shown below. The table also shows how many instructions of a given class are in the program, as a percentage. E.g., if there are 100 instructions in total, there are 60 Class A instructions.

Instruction Class	Computer M1 (Cycles Per Instruction Class)	Computer M2 (Cycles Per Instruction Class)	Percentage of total instruction
A	1	2	60%
B	2	3	30%
C	4	4	10%

Calculate the average **CPI** (Clocks Cycles per Instruction) for computer M1 and M2.

Question 9. (3 points)

Write the MIPS assembly language instructions for the following C statement. Assume f is stored in $s0, g in $s1, h in $s2 and i in $s3. Use **a minimal number of MIPS statements** and **a minimal number of registers**. Remember that MIPS instructions are of the following format : InstructionName R1, R2, R3 where R3 and R2 are source registers and R1 is a destination register.

f = i - (g + h)

Question 10. (2 points)

Perform the following operation by converting the numbers to 16 – bit binary numbers. Use 2's complement for subtraction.

7 - 6

Question 11. (4 points)

Consider the datapath shown in Figure 1. Assume that the processor has only one type of instruction: the 'conditional' jump instruction that executes a jump relative to the address in PC (Program Counter) after comparing register values. Also, assume that there is NO pipelining. Consider that the logic blocks have the latencies as shown in Table 1. Other units have negligible latencies.

(i) Which units in the data-path are used? (2 points)
(ii) What would be the cycle-time for this datapath? (2 points)

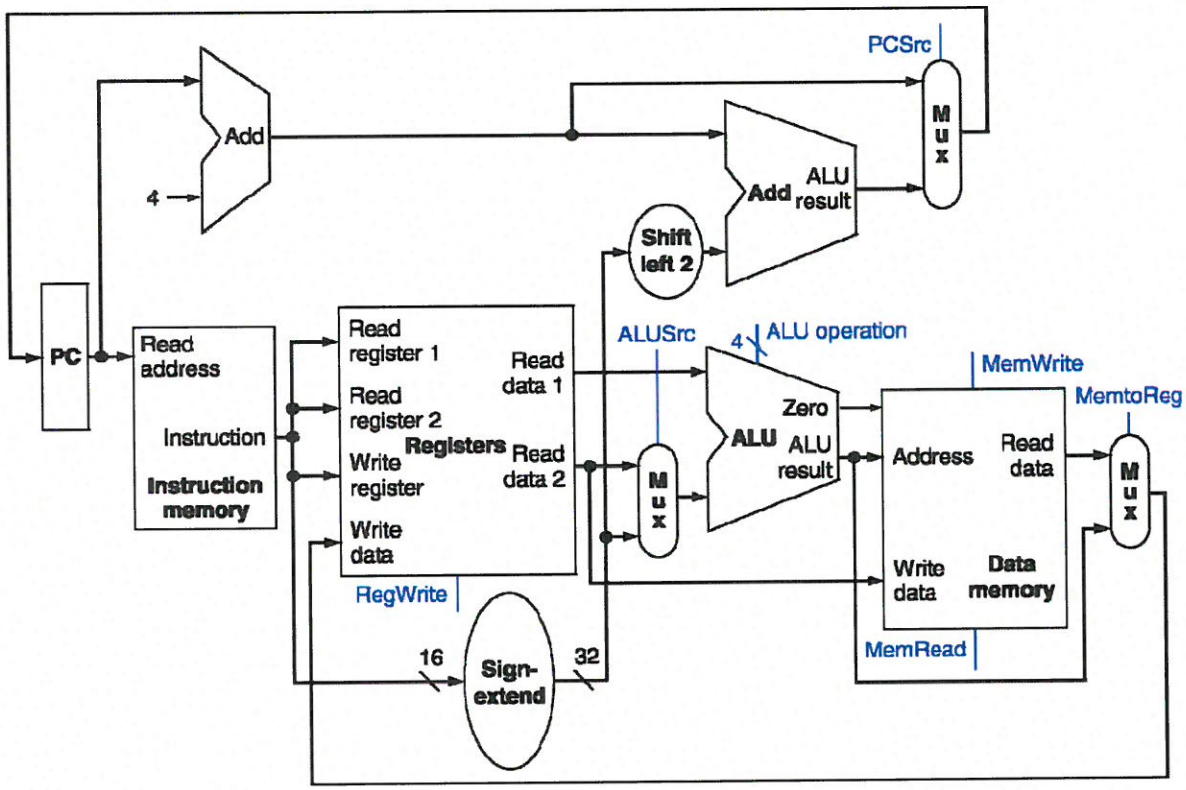

FIGURE 1

I-Mem	ADD	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2
200 ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

TABLE 1

Question 12. (2 points)

In this question, assume that all branches are perfectly predicted (this eliminates all control hazards). Assume, we have only one memory (for both instructions and data), and there might be a structural hazard. To resolve this, the pipeline must be stalled in some cycles.

(i) Show the pipelined execution for each instruction. (1 point)
(ii) Identify and explain where the pipeline stalls. (1 point)

```
        SW   R2,  0(R3)
        OR   R1,  R2,  R3
        BEQ  R2,  R0,  Label  (Assume R2== R0)
        OR   R2,  R2,  R0
Label : ADD  R1,  R4,  R3
```

Question 13. (2 points)

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

The individual stages of the datapath have the latencies as shown above.

(i) Assume a non-pipelined processor. What is the clock cycle time? (1 point)
(ii) Assume a pipelined processor. What is the clock cycle time? (1 point)

Question 14. (3 points)

Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. The processor has a CPI (clock cycles per instruction) of 2 without any memory stalls. Assume that the miss penalty is 100 cycles for each cache-miss. Determine the total CPI of the processor when memory stalls are considered given that frequency of all load and stores is 36%. In your answer, show how the misses due to the instruction cache and the misses due to the data cache contribute to the total CPI.