Försättsblad till skriftlig tentamen vid Linköpings Universitet

Datum för tentamen	2014-01-16
Sal (1) Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och ringa in vilken sal som avses	U14 U15
Tid	8-12
Kurskod	TDTS08
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Datorarkitektur Skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	13
Jour/Kursansvarig Ange vem som besöker salen	Zebo Peng
Telefon under skrivtiden	0702582067
Besöker salen ca kl.	10:00
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Liselotte Lundberg, tel 281278, liselotte.lundberg@liu.se
Tillåtna hjälpmedel	Engelsk ordbok
Övrigt	
Vilken typ av papper ska användas, rutigt eller linjerat	rutigt
Antal exemplar i påsen	

TEKNISKA HÖGSKOLAN I LINKÖPING
Institutionen för datavetenskap (IDA)
Zebo Peng

Tentamen i kursen

TDTS08 Datorarkitektur

(Examination on TDTS 08 Advanced Computer Architecture)

2014-01-16, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs 21 poäng.

Points:

Maximum points: 40.
You need 21 points to pass the exam.

Jourhavande lärare (Teacher on duty):

Zebo Peng, tel. 070 258 2067, 013-28 2067

Note: You can give the answers in English or Swedish.

1. a) There are several write policies that are used to keep the cache contents and the contents of the main memory consistent. Describe briefly each of these policies and discuss the advantages and disadvantages of each of them, respectively.

   b) Describe the additional problems we have when applying these policies in a multiprocessor system.

   (3p)

2. The following sequence of virtual page numbers is encountered in the course of execution on a computer with virtual memory:

   7 5 4 5 4 2 3 6 4 7 1 2 1 7

   Assume that the least-recently used (LRU) page replacement policy is used. Assume also that the main memory has four page frames, and is initially empty. How many page misses will be during this execution? Which are the virtual pages in the main memory when this execution finishes? (3p)

3. We have discussed a technique called forwarding (bypassing) in the context of instruction pipelining.

   a) Describe the basic idea of this technique.

   b) What problem does this technique solve? Why is it important to solve this problem?

   (3p)

4. For the following code, identify the variables that will exhibit temporal locality and the variables that will exhibit spatial locality.

```
for (i = 0; i<100; i++)
   for (j=1000; j>0; j--)
      A[i][j] = A[i][j] + 100;
```

   You should give the reason for your answer (Note: it is not enough to only say which variable has which locality property; you should also explain why).

   (2p)

5. The design of RISC architectures is based on certain characteristics of program execution.

   a) What are the characteristics related to procedure calls and returns?

   b) What is the mechanism used in a RISC architecture to make procedure calls and returns efficient? How does this mechanism work?

   (3p)

Note: You can give the answers in English or Swedish.

6. a) Most of superscalar architectures have a "commit" mechanism. How does this mechanism work? Why do we have it?

   b) If you have a superscalar architecture without the "commit" mechanism, what will be the consequence? What will be the main problem the architecture will suffer?

   (3p)

7. a) Draw a picture to show a typical VLIW architecture.

   b) A VLIW architecture is said to support explicit parallel instruction execution. Define the concept of explicit parallelism. What are the advantages of exploiting explicit parallelism?

   c) What is the main problem of a traditional VLIW computer? How is this problem addressed by the IA-64 architecture?

   (4p)

8. a) What is a vector processor? Draw the block diagram of a typical vector processor architecture.

   b) What is the role of the mask register in a vector unit? Give an example to illustrate the use of the mask register.

   (3p)

9. a) Describe one technique to enforce cache coherence in multiprocessor systems by software solutions.

   b) Discuss the advantages and disadvantages of the proposed technique, respectively.

   (3p)

10. a) Describe the different multithreading approaches and discuss how they are applied in the context of a superscalar architecture. What are the advantages and disadvantages of these different approaches, respectively?

    b) Why does multithreading improve system performance even in the case when there is only a single scalar processor in your computer?

    (3p)

Note: You can give the answers in English or Swedish.

11. a) One argument for using a graphics processing unit (GPU) is that it is power efficient. Describe all features of a GPU architecture that contribute to the reduction of power consumption.

    b) Can we use GPUs for non-graphics computation? Support your answer with some good arguments.

    (3p)

12. a) The dynamic power consumption for CMOS circuits is determined by three parameters, and therefore we have three degrees of freedom in the space for low-power design. What are these three parameters?

    b) For each of these parameters, describe one technique which is most efficient, in your opinion, to achieve low-power design. Explain why you think the described technique is most efficient. (Note: You should present only one technique for each parameter; discussing more than one technique for a give parameter will receive no point).

    (4p)

13. We have discussed several techniques to reduce power consumption of processor cores. One of them is called pipeline gating.

    a) What does it mean by pipeline gating?

    b) Describe one way to implement the pipeline gating technique.

    (3p)