TEKNISKA HÖGSKOLAN I LINKÖPING
Institutionen för datavetenskap (IDA)
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Tentamen i kursen

TDTS08 Datorarkitektur

(Examination on TDTS 08 Advanced Computer Architecture)

2012-08-22, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs 21 poäng.

Points:

Maximum points: 40.
You need 21 points to pass the exam.

Jourhavande lärare (Teacher on duty):

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Note: You can give the answers in English or Swedish.

1. What are the most important issues to be considered when designing the instruction set for a computer architecture? Explain in which way each of these issues has an impact on the performance of the computer. (3p)

2. a) For fully-associative mapping in a cache system, a main memory address is viewed as consisting of two fields. Define these two fields, and explain how they are used.

   b) What are the differences between fully-associative mapping and set-associative mapping? Why is set-associative mapping usually used?

   (3p)

3. a) Why is instruction pipeline widely used to enhance performance of modern computers?

   b) In general, a larger number of pipeline stages gives better performance. However, when the number of stages is becoming very large, the efficiency of the pipeline will not be further improved. Why? Discuss the different issues that prevent the number of pipeline stages to go beyond a certain limit.

   (3p)

4. The design of RISC architectures is based on certain characteristics of program execution.

   a) What are the characteristics concerning procedure calls and returns?

   b) What is the mechanism used in a RISC architecture to make procedure calls and returns efficient? How does this mechanism work?

   (3p)

5. a) What does it mean by static branch prediction? Give an example of a static branch prediction method.

   b) What are the advantages and disadvantages of static branch prediction, as compared to dynamic branch prediction?

   (3p)

6. A microprogrammed control unit is commonly used in a CISC computer to control the execution of the complex instructions. The execution of a complex instruction consisting of several operations in microcode is much faster than the execution of these operations as several machine instructions. Why? Give a simple example to support your argument.

   (3p)

Note: You can give the answers in English or Swedish.

7. a) Identify all the true data dependencies, output dependencies and anti-dependencies on the following code. Provide the reasons for your answers.

```
L2: move r3,r9        Note: r3 <- r9
    load r8,(r3)      Note: r8 <- memory location pointed by r3
    add r3,r3,4       Note: r3 <- r3 + 4
    load r9,(r3)      Note: r9 <- memory location pointed by r3
    ble r8,r9,L3      Note: branch to L3 if r8 less than/equal r9
```

b) Which of the identified dependencies can be eliminated? How?

(3p)

8. a) Draw a picture to show a typical VLIW architecture.

b) A VLIW architecture is said to support explicit parallel instruction execution. Define the concept of explicit parallelism. What are the advantages of exploiting explicit parallelism?

c) What is the main problem of a VLIW computer? How is this problem addressed by the IA-64 architecture?

(4p)

9. a) Define the concept of loop unrolling. Why is loop unrolling very useful in the context of a VLIW processor?

b) Use an example to illustrate how loop unrolling is used in a VLIW processor.

(3p)

10. a) Why is the placement of the "load from memory" operations an important issue for performance?

b) Describe the speculative loading technique. What are the advantages of this technique?

c) Illustrate the speculative loading technique with a simple example.

(3p)

11. a) How are the parallel architectures classified according to Flynn?

b) Describe and draw a diagram for each of the architectures which have been implemented.

c) What are the main factors of a program that limit the speedup by a parallel architecture?

(3p)

Note: You can give the answers in English or Swedish.

12. How are the x86 instructions translated into VLIW instructions in the case of the Crusoe processor? Describe the features of this translation process and the main mechanism used in Crusoe to speed up the execution of the translated code. (3p)

13. a) What is a thread? What does it mean by thread-level parallelism?

b) Describe the different multithreading approaches and discuss how they are applied in the context of superscalar architectures. What are the advantages and disadvantages of these different approaches, respectively?

(3p)