Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2010-08-25
Sal	
Tid	8-12
Kurskod	TDTS08
Provkod	
Kursnamn/benämning	Datorarkitektur
Institution	IDA
Antal uppgifter som ingår i tentamen	13
Antal sidor på tentamen (inkl. försättsbladet)	5
Jour/Kursansvarig	Zhiyuan He
Telefon under skrivtid	0762354600 / 282691
Besöker salen ca kl.	9:30
Kursadministratör (namn + tfnnr + mailadress)	
Tillåtna hjälpmedel	Engelsk ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	

TEKNISKA HÖGSKOLAN I LINKÖPING
Institutionen för datavetenskap
Zebo Peng

Tentamen i kursen

TDTS08 Datorarkitektur

(Examination on TDTS 08 Advanced Computer Architecture)

2010-08-25, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs 21 poäng.

Points:

Maximum points: 40.
You need 21 points to pass the exam.

Jourhavande lärare (Teacher on duty):

Zhiyuan He, tel. 013-28 26 91 / 076-235 46 00

Note: You can give the answers in English or Swedish.

1. What are the most important issues to be considered when designing an instruction set for a computer architecture? Explain in which way each of these issues has an impact on the performance of the computer.

(3p)

2. A computer has a cache, a main memory, and a disk used for virtual memory. If a referenced word is in the cache, 20 *ns* are required to access it. If it is in the main memory but not in the cache, 60 *ns* are needed to load it into the cache, and then the reference is started again. If the word is not in the main memory, 12 *ms* are required to fetch the word from the disk to the main memory, followed by 60 *ns* to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main memory hit ratio is 0.6. What is the average time in *ns* required to access a referenced word in this system?

(2p)

3. a) Why is instruction pipeline widely used to enhance performance of modern computers?

b) In general, a larger number of pipeline stages gives better performance. However, when the number of stages is becoming very large, the efficiency of the pipeline will not be further improved. Why? Discuss the different issues that prevent the number of pipeline stages to go beyond a certain limit.

(3p)

4. The design of RISC architectures is based on certain characteristics of program execution.

a) What are the characteristics concerning procedure calls and returns?

b) What is the mechanism used in a RISC architecture to make procedure calls and returns efficient? How does this mechanism work?

(3p)

5. What are the differences between the superscalar and superpipelined approaches? Compare these two approaches to each other, and discuss their advantages and disadvantages, respectively.

(2p)

Note: You can give the answers in English or Swedish.

6. a) Identify all the true data dependencies, output dependencies and anti-dependencies on the following code. Provide the reasons for your answers.

```
L2: move r3,r7        Note: r3 <- r7
    load r8,(r3)      Note: r8 <- memory location pointed by r3
    add r3,r3,4       Note: r3 <- r3 + 4
    load r9,(r3)      Note: r9 <- memory location pointed by r3
    ble r8,r9,L3      Note: branch to L3 if r8 less than/equal r9
```

b) Which of the identified dependencies can be eliminated? How?

(3p)

7. a) Draw a picture to show a typical VLIW architecture.

b) A VLIW architecture is said to support explicit parallel instruction execution. Define the concept of explicit parallelism. What are the advantages of exploiting explicit parallelism?

c) What is the main problem of a VLIW computer? How is this problem addressed by the IA-64 architecture?

(4p)

8. a) Why is the placement of the "load from memory" operations an important issue?

b) Describe the speculative loading technique. What are the advantages of this technique?

c) Illustrate the speculative loading technique with a simple example.

(3p)

9. a) How are the parallel architectures classified according to Flynn?

b) Describe and draw a diagram for each of the architectures which have been implemented.

c) What are the main factors of a program that limit the speedup by a parallel architecture?

(3p)

10. a) Describe the concept and main features of a computer cluster.

b) What are the main advantages of using a computer cluster?

c) Discuss the features of the two typical configurations of a computer cluster, respectively.

(3p)

Note: You can give the answers in English or Swedish.

11. a) There are two basic approaches to implement a snoopy protocol: write-invalidate and write-update. How do they work, respectively?

b) Describe the situation when the write-invalidate approach works better, and the situation when the write-update works better, respectively.

c) Both these approaches suffer from false sharing overheads. What does it mean by false sharing here?

(4p)

12. How are the x86 instructions translated into VLIW instructions in the case of the Crusoe processor? Describe the features of this translation process and the main mechanism used in Crusoe to speed up the execution of the translated code. (3p)

13. a) What is a thread? What does it mean by thread-level parallelism?

b) Describe the different multithreading approaches and discuss how they are applied in the context of superscalar architectures. What are the advantages and disadvantages of these different approaches, respectively?

c) Why does multithreading improve system performance even in the case when there is only a single scalar processor inside your computer?

(4p)