LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2019-03-20, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Rouhollah Mahfouzi, tel. 013-28 16 31

Good luck !!!

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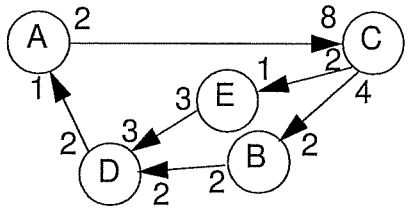
Du kan skriva på svenska eller engelska!

1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

   (3)

2. a) Define synchronous dataflow models.
   Consider the synchronous dataflow graph depicted below.
   b) Find the (minimum) number of firings, for each task, during one period.
   c) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
   d) What is the total buffer space needed (in number of tokens) if (1) the buffer space on the different links is shared; (2) the buffer space on the different links is NOT shared.



   (4p)

3. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

   (2p)

4. a) Are Petri Net models deterministic?
   b) Consider the model in Fig 1a). Which are the possible next states of the Petri Net? Can the place *S* eventually be marked? Is it guaranteed to be marked?
   c) Consider the model in Fig. 1b). Indicate an initial marking of the place *P* such that the place *S* eventually can be marked. Will this guarantee that *S* eventually is marked?

   (3p)

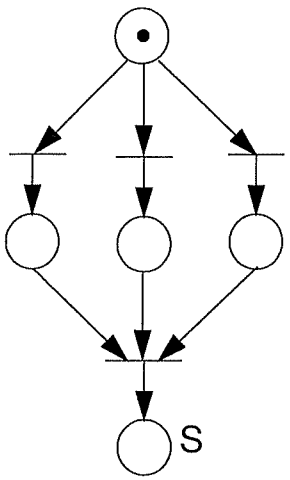


Fig. 1a

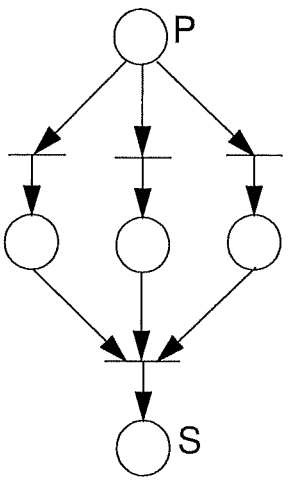


Fig. 1b

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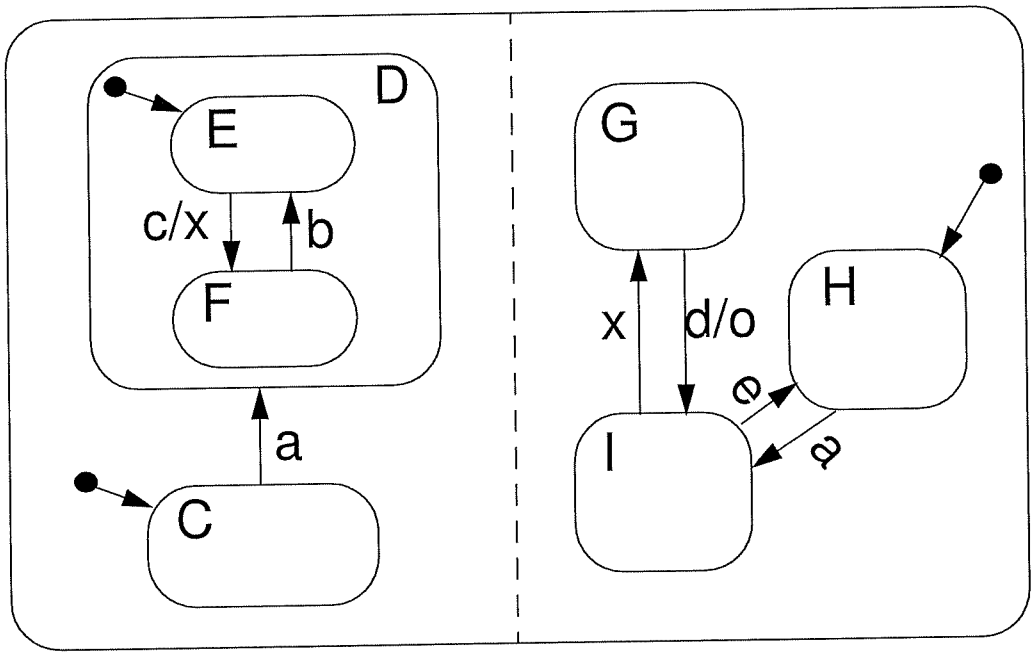
5. How does a discrete event simulator work?
Illustrate by a flow-graph.

(2p)

6. Consider the hierarchical concurrent FSM below. Initial states are indicated by the following sign: ●→. Hence, initially the FSM is in the state C and H. Assume the following sequence of events: a, c, d, b. Indicate the state of the model after each of the four events.



(3)

7. Timed automata are a particular (the simplest) form of hybrid automata. Give an example of a timed automata model of your choice. Explain the model. Specify the same model as hybrid automata.

(2p)

8. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.

(2p)

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9. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

10. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

11. a) What is the basic principle for task scheduling on DVS processors?
    b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
    c) How do we solve the problem that only discrete voltage levels are available?

(3p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

(2p)