

LINKÖPINGS TEKNISKA HÖGSKOLA  
Institutionen för datavetenskap  
Petru Eles

**Tentamen i kursen**  
**Embedded Systems Design - TDDI08**  
**2017-06-09, kl. 08-12**

**Hjälpmedel:**

Engelsk ordbok.

**Supporting material:**

English dictionary.

**Poänggränser:**

Maximal poäng är 30.  
För godkänt krävs sammanlagt  
16 poäng.

**Points:**

Maximum points: 30.  
In order to pass the exam you need a  
total of minimum 16 points.

**Jourhavande lärare:**

Petru Eles, tel. 0703681396

**Good luck !!!**

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**Du kan skriva på svenska eller engelska!**

1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.  
 b) Give short comments on the design steps which belong to the system-level.  
 c) Why is the proposed design flow better than the traditional one?

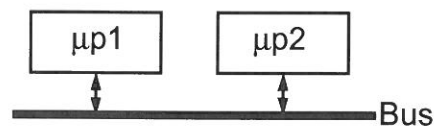
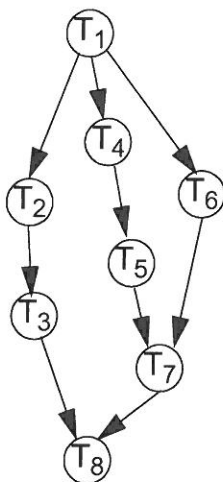
(3)

2. Consider an application modelled as the task graph below. Each task, when activated, consumes one message on each input edge and generates, at termination, one message on each output edge. The task graph is executed on the architecture shown in the figure. Execution times of the tasks, when executed on the corresponding processor, are shown in the table. All messages transmitted over the bus, between tasks mapped on different processors, consume 2 time units to reach the destination. Communication between tasks mapped to the same processor is considered to not consume any time.

Propose an efficient task mapping (indicate on which processor each task is executed) and a corresponding static (nonpreemptive) schedule for the application. Illustrate your schedule as a Gantt chart (similar to the way we captured schedules in Lecture 1&2).

Try to achieve a maximum delay (the time interval between the start of T1 and the finishing of T7) of 46 time units!

(3p)

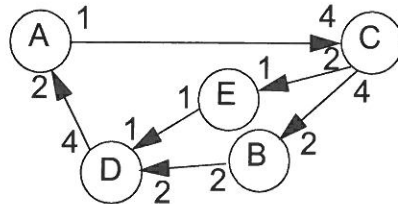


Task	WCET	
	μp1	μp2
T <sub>1</sub>	5	6
T <sub>2</sub>	8	10
T <sub>3</sub>	4	5
T <sub>4</sub>	5	6
T <sub>5</sub>	3	4
T <sub>6</sub>	10	11
T <sub>7</sub>	17	21
T <sub>8</sub>	10	14

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3. Consider the synchronous dataflow graph depicted below.
  - a) Find the (minimum) number of firings, for each task, during one period.
  - b) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
  - c) What is the total buffer space needed (in number of tokens) if (1) the buffer space on the different links is shared; (2) the buffer space on the different links is NOT shared.

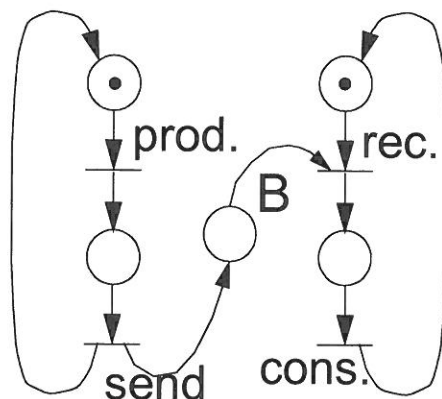


(3p)

4. Define Kahn process networks and synchronous dataflow models. Give an example of a Kahn process network. Show that it cannot be statically scheduled. Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

(3p)

5. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



- a) Is this Petri Net model bounded?
- b) How large is the buffer?
- c) Which transitions are enabled in this state of the model and why?
- d) Draw a similar model in which the buffer has a dimension of four slots.

(3p)

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6. How does a discrete event simulator work?  
Illustrate by a flow-graph.

(2p)
  
7. Timed automata are a particular (the simplest) form of hybrid automata. Give an example of a timed automata model of your choice. Explain the model. Specify the same model as hybrid automata.

(2p)
  
8. What does it mean by an Application Specific Instruction Set Processor (ASIP)?  
We have discussed five dimensions of specialization for ASIPs. Which are those five?  
Comment on each of them.

(2p)
  
9. Describe a simple design flow for processor specialization. Illustrate also by a figure.  
Comment on the design tools you need.

(2p)
  
10. What does it mean by IP (core) based design? What types of cores can you choose from?  
Comment on each of them.

(2p)
  
11. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)
  
12. a) What is the basic principle for task scheduling on DVS processors?  
b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?  
c) How do we solve the problem that only discrete voltage levels are available?  
d) Discuss what the problems are if leakage energy is ignored.

(3p)