LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2017-03-15, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2017-03-15, kl. 14-18
Du kan skriva på svenska eller engelska!

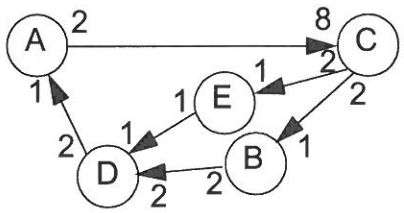
1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

   (3)

2. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

   (2p)

3. Consider the synchronous dataflow graph depicted below.
   a) Find the (minimum) number of firings, for each task, during one period.
   b) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
   c) What is the total buffer space needed (in number of tokens) if (1) the buffer space on the different links is shared; (2) the buffer space on the different links is NOT shared.



   (3p)

4. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

   (3p)

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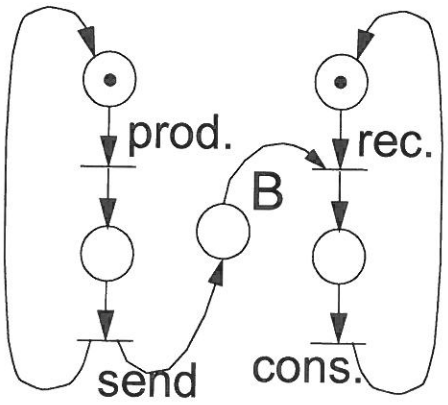
5. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



a) Is this Petri Net model bounded?
b) How large is the buffer?
c) Which transitions are enabled in this state of the model and why?
d) Draw a similar model in which the buffer has a dimension of four slots.

(3p)

6. What is the problem with discrete event simulators and zero delay components? How can it be solved?
Illustrate by an example.

(3p)

7. Timed automata are a particular (the simplest) form of hybrid automata. Give an example of a timed automata model of your choice. Explain the model. Specify the same model as hybrid automata.

(2p)

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8. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
   We have discussed five dimensions of specialization for ASIPs. Which are those five?
   Comment on each of them.

   (3p)

9. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.

   (2p)

10. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

    (2p)

11. a) Formulate the scheduling problem for a set of real-time tasks.
    b) What does it mean that a task set is schedulable?
    c) What does it mean by preemptive and non-preemptive scheduling?

    (2p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

    (2p)