

Försättsblad till skriftlig tentamen vid Linköpings universitet



Datum för tentamen	2016-06-10
Sal (1)	TER4
Tid	8-12
Kurskod	TDDI08
Provkod	TEN1
Kursnamn/benämning Provnamn/benämning	Konstruktion av inbyggda system En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	12
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	0703681396
Besöker salen ca klockan	10:00
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Elin Brödje, 4767, Elin.Brodje@liu.se
Tillåtna hjälpmedel	Engelsk ordbok
Övrigt	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen
Embedded Systems Design - TDDI08
2016-06-10, kl. 8-10

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt
16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a
total of minimum 16 points.

Jourhavande lärare:

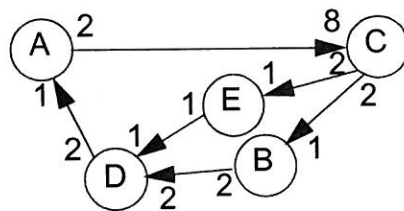
Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2016-06-10, kl. 8-12
Du kan skriva på svenska eller engelska!

1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
 b) Give short comments on the design steps which belong to the system-level.
 c) Why is the proposed design flow better than the traditional one? (3)

2. a) Define synchronous dataflow models.
 Consider the synchronous dataflow graph depicted below.
 b) Find the (minimum) number of firings, for each task, during one period.
 c) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
 d) What is the total buffer space needed (in number of tokens); assume that the buffer space on the different links is shared.



(4p)

3. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
 b) Under which assumptions can we correctly implement a synchronous FSM model? (2p)

4. a) Are Petri Net models deterministic?
 b) Consider the model in Fig 1a). Which are the possible next states of the Petri Net? Can the place *S* eventually be marked? Is it guaranteed to be marked?
 c) Consider the model in Fig. 1b). Indicate an initial marking of the place *P* such that the place *S* eventually can be marked. Will this guarantee that *S* eventually is marked?

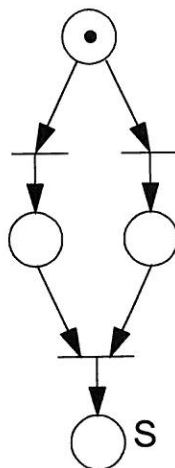


Fig. 1a

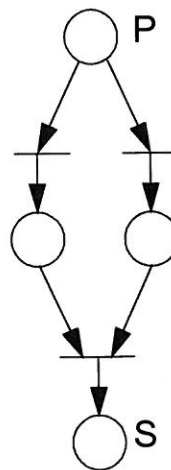


Fig. 1b

(3p)

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5. What is the problem with discrete event simulators and zero delay components? How can it be solved?
Illustrate by an example. (3p)
6. Timed automata are a particular (the simplest) form of hybrid automata. Give an example of a timed automata model of your choice. Explain the model. Specify the same model as hybrid automata. (2p)
7. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
We have discussed five dimensions of specialization for ASIPs. Which are those five?
Comment on each of them. (3p)
8. Describe a simple design flow for processor specialization. Illustrate also by a figure.
Comment on the design tools you need. (2p)
9. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapath can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation? (2p)
10. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor. (2p)
11. What does it mean by IP (core) based design? What types of cores can you choose from?
Comment on each of them. (2p)
12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain. (2p)

