Försättsblad till skriftlig tentamen vid Linköpings universitet

Datum för tentamen	2015-06-11
Sal (1)	TER1
Tid	8-12
Kurskod	TDDI08
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Konstruktion av inbyggda system En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	12
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	0703681396
Besöker salen ca klockan	10
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Carita Lilja, 1463
Tillåtna hjälpmedel	Ordbok
Övrigt	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2015-06-11, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

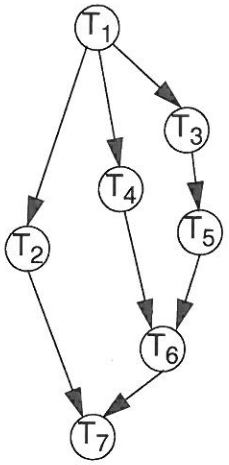
Tentamen i kursen Embedded Systems Design - TDDI08, 2015-06-11, kl. 8-12
Du kan skriva på svenska eller engelska!

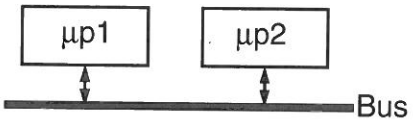
1. Consider an application modelled as the task graph below. Each task, when activated, consumes one message on each input edge and generates, at termination, one message on each output edge. The task graph is executed on the architecture shown in the figure. Execution times of the tasks, when executed on the corresponding processor, are shown in the table. All messages transmitted over the bus, between tasks mapped on different processors, consume 2 time units to reach the destination. Communication between tasks mapped to the same processor is considered to not consume any time.

   Propose an efficient task mapping (indicate on which processor each task is executed) and a corresponding static (nonpreemptive) schedule for the application. Illustrate your schedule as a Gantt chart (similar to the way we captured schedules in Lecture 1&2).

   Try to achieve a maximum delay (the time interval between the start of T1 and the finishing of T7) of 46 time units!

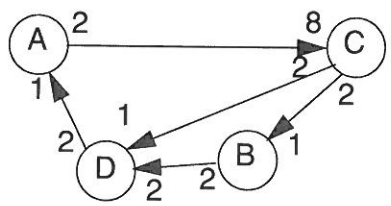
   (3p)





Task	WCET	
	µp1	µp2
T_1	5	6
T_2	12	15
T_3	5	6
T_4	8	10
T_5	5	5
T_6	17	21
T_7	10	14

2. Consider the synchronous dataflow graph depicted below.
   a) Find the (minimum) number of firings, for each task, during one period.
   b) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
   c) What is the total buffer space needed (in number of tokens); assume that the buffer space on the different links is not shared.



   (3p)

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3. Give an example and show how determinism is lost with a GALS model as opposed to a synchronous FSM.

(2p)

4. Define Kahn process networks and synchronous dataflow models.
Give an example of a Kahn process network. Show that it cannot be statically scheduled.
Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

(3p)

5. a) Are Petri Net models deterministic?
b) Consider the model in Fig 1a). Can the place *S* eventually be marked? Is it guaranteed to be marked?
c) Consider the model in Fig. 1b). Starting with the marking in the figure, which is (are) the possible next state(s) of the system? Can the place *S* eventually be marked? Is it guaranteed to be marked?

(3p)

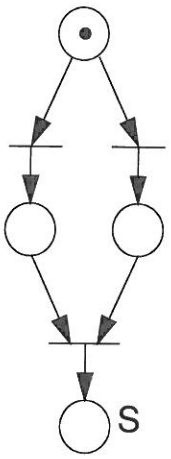

Fig. 1a

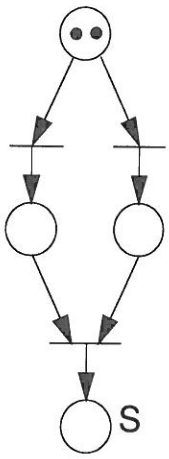

Fig. 1b

6. How does a discrete event simulator work?
Illustrate by a flow-graph.

(2p)

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7. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapth can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation?

(2p)

8. We have introduced three particular policies for shut-down with Dynamic Power Management: time-out, predictive, and stochastic. Describe the main characteristics of each. Compare.

(2p)

9. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.

(3p)

10. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

11. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

12. a) What is the basic principle for task scheduling on DVS processors?
    b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
    c) How do we solve the problem that only discrete voltage levels are available?
    d) Discuss what the problems are if leakage energy is ignored.

(3p)