LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2015-03-21, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt
16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

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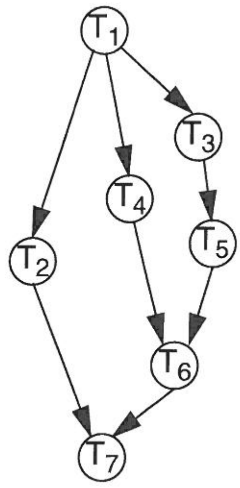
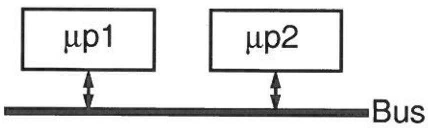
Du kan skriva på svenska eller engelska!

1. Consider an application modelled as the task graph below. Each task, when activated, consumes one message on each input edge and generates, at termination, one message on each output edge. The task graph is executed on the architecture shown in the figure. Execution times of the tasks, when executed on the corresponding processor, are shown in the table. All messages transmitted over the bus, between tasks mapped on different processors, consume 2 time units to reach the destination. Communication between tasks mapped to the same processor is considered to not consume any time.
   Propose an efficient task mapping (indicate on which processor each task is executed) and a corresponding static (nonpreemptive) schedule for the application. Illustrate your schedule as a Gantt chart (similar to the way we captured schedules in Lecture 1&2).
   Try to achieve a maximum delay (the time interval between the start of T1 and the finishing of T7) of 46 time units!

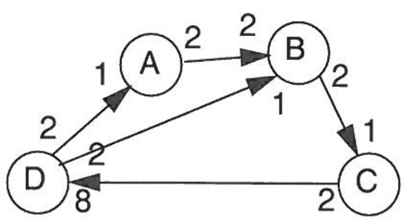
(3p)





Task	WCET	
	µp1	µp2
T_1	5	6
T_2	12	15
T_3	5	6
T_4	8	10
T_5	5	5
T_6	17	21
T_7	10	14

2. Consider the synchronous dataflow graph depicted below.
   a) Find the (minimum) number of firings, for each task, during one period.
   b) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle)
   c) What is the total buffer space needed (in number of tokens); assume that the buffer space on the different links is not shared.



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(3p)

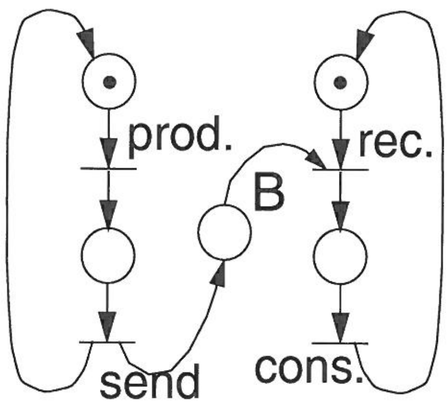
3. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

(2p)

4. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

(3p)

5. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



   a) Is this Petri Net model bounded?
   b) How large is the buffer?
   c) Which transitions are enabled in this state of the model and why?
   d) Draw a similar model in which the buffer has a dimension of four slots.

(3p)

6. What is the problem with discrete event simulators and zero delay components? How can it be solved?
   Illustrate by an example.

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(3p)

7. We have introduced three particular policies for shut-down with Dynamic Power Management: time-out, predictive, and stochastic. Describe the main characteristics of each. Compare.

(2p)

8. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
We have discussed five dimensions of specialization for ASIPs. Which are those five?
Comment on each of them.

(3p)

9. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

10. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

11. a) What is the basic principle for task scheduling on DVS processors?
b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
c) How do we solve the problem that only discrete voltage levels are available?

(2p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

(2p)