Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2014-06-12
Sal	TER 2
Tid	8 - 12
Kurskod	TDDI08
Provkod	TEN1
Kursnamn/benämning	Konstruktion av inbyggda system
Institution	*IDA*
Antal uppgifter som ingår i tentamen	12
Antal sidor på tentamen (inkl. försättsbladet)	
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	0703681396
Besöker salen ca kl.	10:00
Kursadministratör (namn + tfnnr + mailadress)	Carita Lilja , 1463, carita.lilja@liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	16

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2014-06-12, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2014-06-12, kl. 8-12
Du kan skriva på svenska eller engelska!

1. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

(2p)

2. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

(3p)

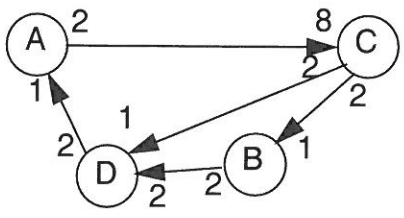
3. Give an example and show how determinism is lost with a GALS model as opposed to a synchronous FSM.

(2p)

4. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

(3p)

5. Consider the synchronous dataflow graph depicted below.
   a) Find the (minimum) number of firings, for each task, during one period.
   b) Elaborate a static schedule (a sequence of task executions that can be repeated in a cycle).



(3p)

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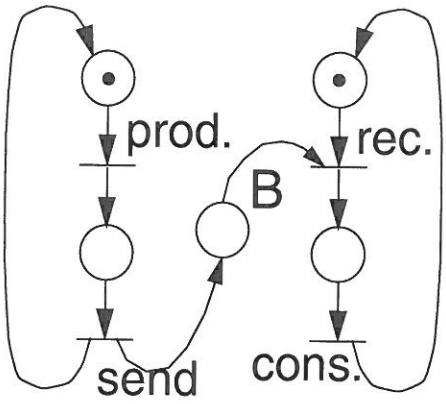
6. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



a) Is this Petri Net model bounded?
b) How large is the buffer?
c) Which transitions are enabled in this state of the model and why?
d) Draw a similar model in which the buffer has a dimension of four slots.

(3p)

7. How does a discrete event simulator work?
Illustrate by a flow-graph.

(2p)

8. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
We have discussed five dimensions of specialization for ASIPs. Which are those five?
Comment on each of them.

(3p)

9. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.

(3p)

10. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

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11. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

(2p)