Försättsblad till skriftlig tentamen vid Linköpings Universitet

Datum för tentamen	2013-06-07
Sal (2) Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och ringa in vilken sal som avses	R41 U15
Tid	8-12
Kurskod	TDDI08
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Konstruktion av inbyggda system En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	12
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	0703681396
Besöker salen ca kl.	10:15
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Carita Lilja, 1463, carita.lilja@.liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2013-06-07, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2013-06-07, kl. 8-12
Du kan skriva på svenska eller engelska!

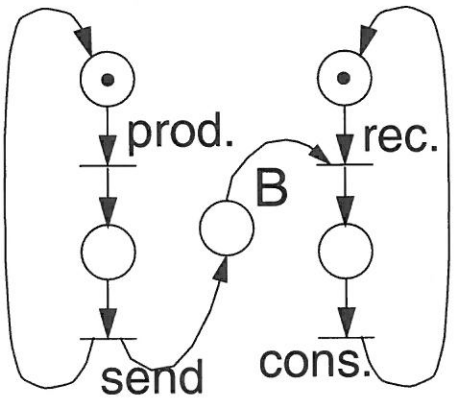
1. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

   (2p)

2. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

   (3p)

3. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



   a) Is this Petri Net model bounded?
   b) How large is the buffer?
   c) Which transitions are enabled in this state of the model and why?
   d) Draw a similar model in which the buffer has a dimension of four slots.

   (3p)

4. Define Kahn process networks.
   Show by an example how determinism is guaranteed with Kahn process networks.
   Transform the example and show that a more general dataflow network, which is not a Kahn process network, does not guarantee determinism.

   (3p)

Tentamen i kursen Embedded Systems Design - TDDI08, 2013-06-07, kl. 8-12
Du kan skriva på svenska eller engelska!

5. Timed automata are a particular (the simplest) form of hybrid automata. Give an example of a timed automata model of your choice. Explain the model. Specify the same model as hybrid automata.

(3p)

6. What is the problem with discrete event simulators and zero delay components? How can it be solved?
Illustrate by an example.

(3p)

7. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.
How does this differ from the design flow for a platform definition?

(3p)

8. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapth can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation?

(2p)

9. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

10. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

11. What is good with static cyclic scheduling? What is bad?

(2p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

(2p)