Försättsblad till skriftlig tentamen vid Linköpings Universitet

Datum för tentamen	2012-08-24
Sal (1) Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och ringa in vilken sal som avses	TER3
Tid	14-18
Kurskod	TDDI08
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Konstruktion av inbyggda system En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	12
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	0703681396
Besöker salen ca kl.	15:30
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Gunilla Mellheden, 282297, gunilla.mellheden@liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2012-08-24, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2012-08-24, kl. 14-18
Du kan skriva på svenska eller engelska!

1. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

   (2p)

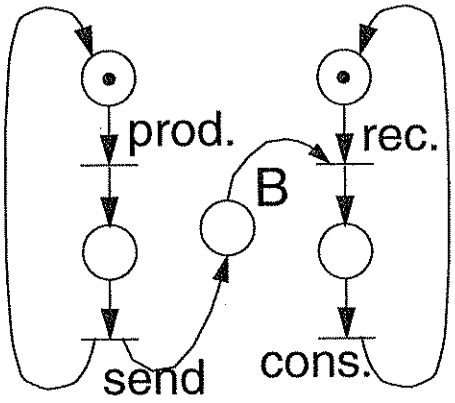
2. a) What does it mean by data-driven and control-driven concurrency?
   b) Give an example for each of them.

   (2p)

3. Give an example and show how determinism is lost with a GALS model as opposed to a synchronous FSM.

   (2p)

4. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



   a) Is this Petri Net model bounded?
   b) How large is the buffer?
   c) Which transitions are enabled in this state of the model and why?
   d) Draw a similar model in which the buffer has a dimension of four slots.

   (3p)

5. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

   (3p)

Tentamen i kursen Embedded Systems Design - TDDI08, 2012-08-24, kl. 14-18
Du kan skriva på svenska eller engelska!

6. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapth can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation?

(3p)

7. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
We have discussed five dimensions of specialization for ASIPs. Which are those five?
Comment on each of them.

(3p)

8. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.
How does this differ from the design flow for a platform definition?

(3p)

9. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

10. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

11. a) Formulate the scheduling problem for a set of real-time tasks.
b) What does it mean that a task set is schedulable?
c) What does it mean by preemptive and non-preemptive scheduling?

(2p)

12. a) What is the basic principle for task scheduling on DVS processors?
b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
c) How do we solve the problem that only discrete voltage levels are available?
d) Discuss what the problems are if leakage energy is ignored.

(3p)