Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2010-08-27
Sal	
Tid	14-18
Kurskod	TDDI08
Provkod	
Kursnamn/benämning	Konstruktion av inbyggda system
Institution	*IDA*
Antal uppgifter som ingår i tentamen	12
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	281396, 0703681396
Besöker salen ca kl.	16
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, 282297, gunilla.mellheden@liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2010-08-27, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 281396, 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2010-08-27, kl. 14-18
Du kan skriva på svenska eller engelska!

1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

   (3p)

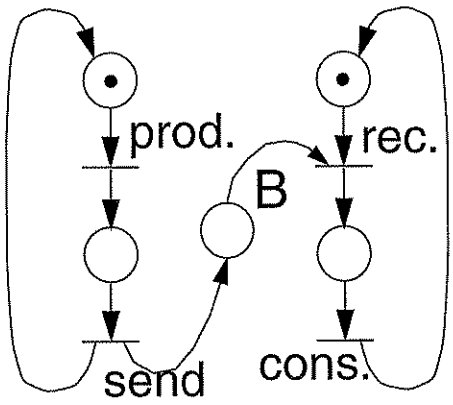
2. Compare reasoning about time with synchronous FSMs and Timed Automata.

   (2p)

3. Give an example and show how determinism is lost with a GALS model as opposed to a synchronous FSM.

   (2p)

4. The figure below represents a Petri Net model for two processes, a producer and a consumer, which are communicating through a buffer; the buffer is represented by place B.



   a) Is this Petri Net model bounded?
   b) How large is the buffer?
   c) Which transitions are enabled in this state of the model and why?
   d) Draw a similar model in which the buffer has a dimension of four slots.

   (3p)

5. How does a discrete event simulator work?
   Illustrate by a flow-graph.

   (2p)

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6. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapth can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation?

(3p)

7. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.
How does this differ from the design flow for a platform definition?

(3p)

8. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

9. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

10. We have introduced three particular policies for shut-down with Dynamic Power Management: time-out, predictive, and stochastic. Describe the main characteristics of each. Compare.

(3p)

11. What is good with static cyclic scheduling? What is bad?

(2p)

12. a) What is the basic principle for task scheduling on DVS processors?
b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
c) How do we solve the problem that only discrete voltage levels are available?
d) Discuss what the problems are if leakage energy is ignored.

(3p)