Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2010-06-11
Sal	
Tid	8-12
Kurskod	TDDI08
Provkod	
Kursnamn/benämning	Embedded Systems Design
Institution	*IDA*
Antal uppgifter som ingår i tentamen	12
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	0703681396
Besöker salen ca kl.	10
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, gunme@ida.liu.se, 2297
Tillåtna hjälpmedel	Ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2010-06-11, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 281396, 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2010-06-11, kl. 8-12
Du kan skriva på svenska eller engelska!

1. Compare reasoning about time with synchronous FSMs and Timed Automata.

(2p)

2. Give an example and show how determinism is lost with a GALS model as opposed to a synchronous FSM.

(2p)

3. a) Are Petri Net models deterministic?
   b) Consider the model in Fig 1a). Starting with the marking in the figure, which is (are) the possible next state(s) of the model? Can the state *S* eventually be reached? Is it guaranteed to be reached?
   c) Consider the model in Fig. 1b). Can the state *S* eventually be reached? Is it guaranteed to be reached?

(3p)

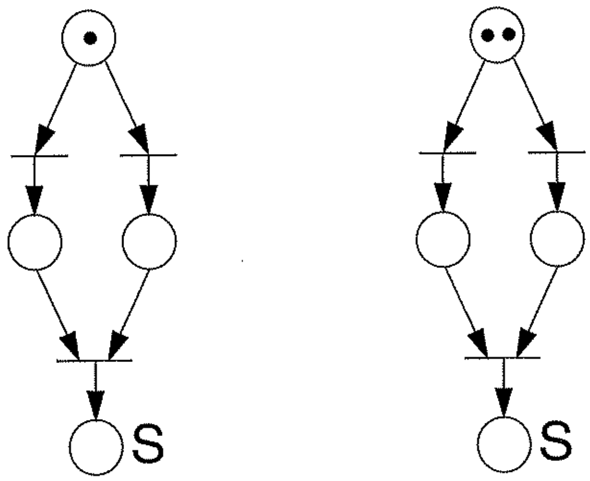

Fig. 1a   Fig. 1b

4. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

(3p)

5. How does a discrete event simulator work?
   Illustrate by a flow-graph.

(2p)

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6. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
We have discussed five dimensions of specialization for ASIPs. Which are those five?
Comment on each of them.

(3p)

7. Describe a simple design flow for processor specialization. Illustrate also by a figure. Comment on the design tools you need.
How does this differ from the design flow for a platform definition?

(3p)

8. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

(2p)

9. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

(2p)

10. We have introduced three particular policies for shut-down with Dynamic Power Management: time-out, predictive, and stochastic. Describe the main characteristics of each. Compare.

(3p)

11. a) Formulate the scheduling problem for a set of real-time tasks.
What does it mean that a task set is schedulable?
b) How does it change if energy optimisation is taken into consideration?
c) What does it mean by preemptive and non-preemptive scheduling?

(3p)

12. Show that, if leakage is ignored, it is possible that, by over-reduction of the supply voltage, the total energy consumption is increased. Use diagrams to explain.

(2p)