Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2010-03-17
Sal	U3, U1
Tid	14-18
Kurskod	TDDI08
Provkod	
Kursnamn/benämning	
Institution	*IDA*
Antal uppgifter som ingår i tentamen	12
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	281396, 0703681396
Besöker salen ca kl.	16
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, 282297, gunme@ida.liu.se
Tillåtna hjälpmedel	ordbuk
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

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LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Embedded Systems Design - TDDI08

2010-03-17, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 30.
För godkänt krävs sammanlagt 16 poäng.

Points:

Maximum points: 30.
In order to pass the exam you need a total of minimum 16 points.

Jourhavande lärare:

Petru Eles, tel. 281396, 0703681396

Good luck !!!

Tentamen i kursen Embedded Systems Design - TDDI08, 2010-03-17, kl. 14-18
Du kan skriva på svenska eller engelska!

1. a) Describe, using a flow graph, the design flow of an embedded systems, from an informal specification to fabrication.
   b) Give short comments on the design steps which belong to the system-level.
   c) Why is the proposed design flow better than the traditional one?

   (3p)

2. a) What does it mean by data-driven and control-driven concurrency?
   b) Give an example for each of them.

   (2p)

3. a) Formulate the synchrony hypothesis for FSMs. What does it imply?
   b) Under which assumptions can we correctly implement a synchronous FSM model?

   (2p)

4. a) Are Petri Net models deterministic?
   b) Consider the model in Fig 1a). Starting with the marking in the figure, which is (are) the possible next state(s) of the model? Can the state *S* eventually be reached? Is it guaranteed to be reached?
   c) Consider the model in Fig. 1b). Can the state *S* eventually be reached? Is it guaranteed to be reached?

   (3p)

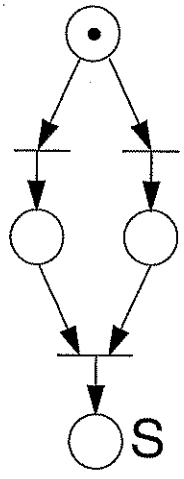

Fig. 1a

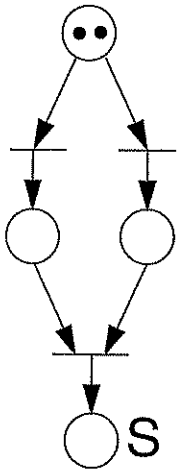

Fig. 1b

5. Define Kahn process networks and synchronous dataflow models.
   Give an example of a Kahn process network. Show that it cannot be statically scheduled.
   Adjust the example such that it becomes a synchronous dataflow model. Show a static schedule for this new model.

   (3p)

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6. What does it mean by an Application Specific Instruction Set Processor (ASIP)?
   We have discussed five dimensions of specialization for ASIPs. Which are those five?
   Comment on each of them.

   (3p)

7. We have introduced Systems on Chip with a dynamically reconfigurable datapath; this datapth can be reconfigured to act as an accelerator for the actual program running on the processor. What are the main steps for compiling the source code for such a system? What will result as the outcome of this compilation?

   (2p)

8. Illustrate by a diagram the trade-off energy consumption vs. flexibility for ASIC, FPGA, ASIP, and general-purpose processor.

   (2p)

9. What does it mean by IP (core) based design? What types of cores can you choose from? Comment on each of them.

   (2p)

10. We have introduced three particular policies for shut-down with Dynamic Power Management: time-out, predictive, and stochastic. Describe the main characteristics of each. Compare.

    (3p)

11. What is good with static cyclic scheduling? What is bad?

    (2p)

12. a) What is the basic principle for task scheduling on DVS processors?
    b) What is the problem if we consider particularities, concerning power consumption, of individual tasks?
    c) How do we solve the problem that only discrete voltage levels are available?
    d) Discuss what the problems are if leakage energy is ignored.

    (3p)