Försättsblad till skriftlig tentamen vid Linköpings universitet

Datum för tentamen	2019-09-07
Sal (2)	TER2(11) TERE(1)
Tid	8-12
Utb. kod	TDDI03
Modul	TEN1
Utb. kodnamn/benämning **Modulnamn/benämning**	Datorarkitektur En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	14
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	013-28 13 96
Besöker salen ca klockan	10:00
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	
Tillåtna hjälpmedel	Engelsk ordbok
Övrigt	
Antal exemplar i påsen	

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LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2019-09-07, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2019-09-07, kl. 8-12
Du kan skriva på svenska eller engelska!

1.

a) Why do we need special *write strategies* for cache memories?

b). We have discussed three write strategies: How do they work? Which are their advantages and disadvantages?

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards.
In what consists the particularity and what is the reason behind it?

(3p)

3. Define the three types of pipeline hazards. Give an example for each.

(3p)

4. Branch history table: what does it contain and how is it used?

(2p)

5. Enumerate five of the main characteristics of RISC architectures.

(2p)

6. Dynamic branch prediction with a two-bit scheme. How does it work?
Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        ----------------
LOOP    ----------------
        ----------------
        BNZ     LOOP
        ----------------
```

(3p)

7.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

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8.

a) Which are the types of data dependencies that have to be considered with an out-of-order superscalar? Give an example for each.

b) Why do we call them "true" and "artificial", respectively?

c) What can be solved by register renamimg? Give an example.

(3p)

9. Compare VLIW architectures with superscalar architectures:

a) Show similarities and differences.

b) Show the advantages and disadvantages of the two approaches.

c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

10. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

11.

a) What is branch predication (like in the Itanium architecture)?

b) Compare with ordinary branch prediction.

(3p)

12. Formulate Amdahl's law and comment.

(3p)

13.

a) What is hardware multithreading?

b) Why do multithreaded processors provide higher performance?

c) We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?

(3p)

14. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)