LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2019-04-23, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

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Good luck !!!

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Du kan skriva på svenska eller engelska!

1. The Pentium 4 has an L1 instruction cache which is particular in several regards.
   In what consists the particularity and what is the reason behind it?

(3p)

2. A two-way set-associative cache has lines of 32 (=2^5) bytes and a total size of 32 Kbytes (=2^{15}). The main memory has a size of 64-Mbyte (=2^{26}). Show the format of main memory addresses (give the total number of address bits, what different groups of address bits indicate, and how long each of these groups is).

(3p)

3.

a) What is the role of the page table in a virtual memory system? What data does it store?
b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

4. Consider a pipelined processor with *k* pipeline stages.

a) What is the theoretical acceleration (ignoring overheads) for a sequence of *n* instructions, compared to a similar but non-pipelined processor? Show how you obtain the formula!
b) What is the acceleration of a sequence of 105 instructions if the number of pipeline stages is 9?
c) What is the acceleration for an infinitely long sequence if the number of pipeline stages is 9?

(3p)

5. Dynamic branch prediction with a two-bit scheme. How does it work?
   Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        - - - - - - - - - - - - - - -
LOOP    - - - - - - - - - - - - - - -
        - - - - - - - - - - - - - - -
        BNZ     LOOP
        - - - - - - - - - - - - - - -
```

(3p)

6. Enumerate five of the main characteristics of RISC architectures.

(2p)

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7. Branch history table: what does it contain and how is it used?

(2p)

8.

a) What is a superscalar architecture?
b) Draw a block-diagram of a superscalar unit.

(3p)

9.

Consider the following sequence of machine instructions:

1. R4 <- R10 + R1
2. R7 <- R5 * 10
3. R11 <- R4 - R0
4. R3 <- R11 - R16
5. R10 <- R7 + 101
6. R9 <- R3 + R12
7. R8 <- R6 * R0
8. R2 <- R3 * R7
9. R13 <- R17 + 2
10. R5 <- R12 * R22
11. R8 <- R5 + 3

a) Indicate the data dependencies among instructions.
b) Rename the registers in the above sequence to prevent, where possible, dependency problems.

(2p)

10. Compare VLIW architectures with superscalar architectures:

a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

11. What is loop unrolling? How does it work? Why is it important with VLIW architectures? Give an example.

(3p)

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12.

a) What is branch predication (like in the Itanium architecture)?

b) Compare with ordinary branch prediction.

(3p)

13. Consider an instruction sequence such that 25% of the computation has to be executed sequentially, while the rest is executed with full parallelism on 6 processors. Calculate the expected speedup and efficiency.

(3p)

14. What is a vector processor? Draw a block diagram.
    What is the role of the mask register?
    What is the basic difference between array processors and vector processors?

(3p)