LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2018-04-03, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 013 281396

Good luck !!!

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Du kan skriva på svenska eller engelska!

1. The Pentium 4 has an L1 instruction cache which is particular in several regards. In what consists the particularity and what is the reason behind it?

(3p)

2. A set-associative cache consists of 512 (=2^8) lines, divided into two-line sets. The main memory contains 128K (=2^{17}) blocks of 128 (=2^7) bytes each. Show the format of the main memory address (give the total number of address bits, what different groups of address bits indicate, and how long each of these groups is).

(3p)

3.

a) What is the role of the page table in a virtual memory system? What is the role of the translation lookaside buffer (TLB)?

(2p)

4. Consider a pipelined processor with k pipeline stages.

a) What is the theoretical acceleration (ignoring overheads) for a sequence of n instructions, compared to a similar but non-pipelined processor? Show how you obtain the formula!

b) What is the acceleration of a sequence of 60 instructions if the number of pipeline stages is 12?

c) What is the acceleration for an infinitely long sequence if the number of pipeline stages is 12?

(3p)

5. Branch history table: what does it contain and how is it used?

(2p)

6. The design of RISC architectures is based on certain characteristics of typical programs which are frequently used. Enumerate at least five such characteristics of programs.

(3p)

7. Delayed load. Why do we need it with RISC architectures? How does it work? Give an example.

(3p)

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8.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

9. Dynamic branch prediction with a two-bit scheme. How does it work?
Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        ----------------
LOOP    ----------------
        ----------------
        BNZ    LOOP
        ----------------
```

(3p)

10. What is loop unrolling? How does it work? Give an example. Why is it important with VLIW architectures?

(3p)

11. Compare VLIW architectures with superscalar architectures:

a) Show similarities and differences.

b) Show the advantages and disadvantages of the two approaches.

c) Why is a superscalar consuming more power, compared to a VLIW computer?

(3p)

12. Consider an instruction sequence such that 40% of the computation has to be executed sequentially, while the rest is executed with full parallelism on 10 processors. Calculate the expected speedup and efficiency.

(3p)

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13. Flynn's Classification of Computer Architectures: Explain and illustrate by figures.

(3p)

14.

a) What is hardware multithreading?
b) Why do multithreaded processors provide higher performance?
c) We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?

(3p)