LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2018-01-11, kl. 08-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt
21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a
total of minimum 21 points.

Jourhavande lärare:

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Good luck !!!

1.
a) Why do we need special *write strategies* for cache memories?
b). We have discussed three write strategies. How do they work? Which are their advantages and disadvantages?

(3p)

2. A set-associative cache consists of 512 ($=2^9$) lines, divided into four-line sets. The main memory contains 128K ($=2^{17}$) blocks of 128 ($=2^7$) bytes each. Show the format of the main memory address (give the total number of address bits, what different groups of address bits indicate, and how long each of these groups is).

(3p)

3.
a) What is the role of the page table in a virtual memory system? What is the role of the translation lookaside buffer (TLB)?

(2p)

4. Consider a pipelined processor with k pipeline stages.
a) What is the theoretical acceleration (ignoring overheads) for a sequence of n instructions, compared to a similar but non-pipelined processor? Show how you obtain the formula!
b) What is the acceleration of a sequence of 100 instructions if the number of pipeline stages is 8?
c) What is the acceleration for an infinitely long sequence if the number of pipeline stages is 8?

(3p)

5. Define the three types of pipeline hazards. Give an example for each.

(3p)

6. The design of RISC architectures is based on certain characteristics of typical programs which are frequently used. Enumerate at least five such characteristics of programs.

(2p)

7.
a) What is a superscalar architecture?
b) Draw a block-diagram of a superscalar unit.

(3p)

8.

Consider the following sequence of machine instructions:

1:	R1	←	R0 + R2
2:	R7	←	R1 + R12
3:	R5	←	R7 - 1
4:	R1	←	R2 * R4
5:	R7	←	R9 + 10
6:	R12	←	R4 - 25
7:	R3	←	R5 * 2
8:	R4	←	R1 + R3
9:	R10	←	R8 - 2
10:	R1	←	R1 * 3

a) Indicate the data dependencies among instructions.

b) Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two units that execute addition&subtraction and one unit for multiplication. Produce a table, according to the model below, showing how instructions are executed in consecutive cycles, if we assume in order execution.

c) Rename the registers in the above sequence to prevent, where possible, dependency problems. Produce a second table, according to the model below, showing how instructions (after register renaming) are executed in consecutive cycles, if we assume out of order execution.

In the table cells indicate the sequence number (1, 2, .., 10) of the instruction executed in the corresponding cycle on the respective unit.

	ADD/SUB	ADD/SUB	MUL
Cycle 1			
Cycle 2			
Cycle 3			
. . .			

(4p)

9. What is trace scheduling? How does it work? Why is it important with VLIW architectures?

(3p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why is a superscalar consuming more power, compared to a VLIW computer?

(3p)

11.
a) What is branch predication (like in the Itanium architecture)?
b) Compare with ordinary branch prediction.

(2p)

12. Consider an instruction sequence such that 40% of the computation has to be executed sequentially, while the rest is executed with full parallelism on 10 processors. Calculate the expected speedup and efficiency.

(3p)

13. Flynn's Classification of Computer Architectures: Explain and illustrate by figures.

(3p)

14. What is a vector processor? Draw a block diagram.
What is the role of the mask register?
What is the basic difference between array processors and vector processors?

(3p)