LINKÖPINGS TEKNISKA HÖGSKOLA Institutionen för datavetenskap Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2016-03-29, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40. För godkänt krävs sammanlagt 21 poäng. **Points:**

Maximum points: 40. In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

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1.		
a) b).	Why do we need special write strategies for cache memories? We have discussed three write strategies: write-through, write through with buffered write, a copy back. How do they work? Which are their advantages and disadvantages?	anc
2.	A set-associative cache consists of 256 ($=2^8$) lines, divided into two-line sets. The mammemory contains 64K ($=2^{16}$) blocks of 128 ($=2^7$) bytes each. Show the format of the mammemory address (give the total number of address bits, what different groups of address b indicate, and how long each of these groups is).	ain
3. a) b) c)	Consider a pipelined processor with k pipeline stages. What is the theoretical acceleration (ignoring overheads) for a sequence of n instruction compared to a similar but non-pipelined processor? Show how you obtain the formula! What is the acceleration of a sequence of 60 instructions if the number of pipeline stages is 1. What is the acceleration for an infinitely long sequence if the number of pipeline stages is 1. (3)	2?
4.	The Pentium 4 has an L1 instruction cache which is particular in several regards. In what consists the particularity and what is the reason behind it?	(p)
5.	The design of RISC architectures is based on certain characteristics of typical programs which are frequently used. Enumerate at least five such characteristics of programs.	
6.	Dynamic branch prediction with a two-bit scheme. How does it work? Illustrate with the case of a loop like the one below. Compare with one-bit prediction. LOOP BNZ LOOP	

(3p)

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1.	
a)	What is a superscalar architecture?
b)	Draw a block-diagram of a superscalar unit. (3p
	(5)
8.	
a)	Which are the types of data dependencies that have to be considered with an out-of-orde superscalar? Give an example for each.
b)	Why do we call them "true" and "artificial", respectively?
c)	What can be solved by register renaming? Give an example. (3p)
	(Sp.
9.	Compare VLIW architectures with superscalar architectures:
a)	Show similarities and differences.
b)	Show the advantages and disadvantages of the two approaches.
c)	Why is a superscalar consuming more power, compared to a VLIW computer?
	(4p)
10.	What is trace scheduling? How does it work (remember the three stees)? Why is it important
10.	What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?
	(3p)
11.	
a)	What is branch predication (like in the Itanium architecture)?
b)	Compare with ordinary branch prediction.
	(3p)
12.	Formulate Amdahl's law and comment.
	(2p)
13.	
a)	What is hardware multithreading?
b)	Why do multithreaded processors provide higher performance?
c)	We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?
	(3p)
14.	What is the role of the mask register in a vector unit? Give an example.
	(3p)