LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2016-01-11, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt
21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a
total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

1.
a) Why do we need special *write strategies* for cache memories?
b). We have discussed three write strategies: *write-through*, *write through with buffered write*, and *copy back*. How do they work? Which are their advantages and disadvantages?

(3p)

2. A set-associative cache consists of 256 ($=2^8$) lines, divided into four-line sets. The main memory contains 32K ($=2^{15}$) blocks of 128 ($=2^7$) bytes each. Show the format of the main memory address (give the total number of address bits, what different groups of address bits indicate, and how long each of these groups is).

(3p)

3. Consider a pipelined processor with k pipeline stages.
a) What is the theoretical acceleration (ignoring overheads) for a sequence of n instructions, compared to a similar but non-pipelined processor? Show how you obtain the formula!
b) What is the acceleration of a sequence of 30 instructions if the number of pipeline stages is 7?
c) What is the acceleration for an infinitely long sequence if the number of pipeline stages is 7?

(3p)

4. Branch history table: what does it contain and how is it used?

(2p)

5. Enumerate five of the main characteristics of RISC architectures.

(2p)

6. Delayed load. Why do we need it with RISC architectures? How does it work? Give an example.

(2p)

7.
a) What is the role of the page table in a virtual memory system? What data does it store?
b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

8.
a) What is a superscalar architecture?
b) Draw a block-diagram of a superscalar unit.

(3p)

9.
Consider the following sequence of machine instructions:

1:	R1	←	R0 + R2
2:	R5	←	R1 + R12
3:	R7	←	R5 + 1
4:	R1	←	R2 * R4
5:	R5	←	R9 + 10
6:	R12	←	R4 - 25
7:	R3	←	R7 * 2
8:	R4	←	R1 + R3
9:	R10	←	R8+22
10:	R1	←	R1 * 30

a) Indicate the data dependencies among instructions.
b) Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two units that execute addition&subtraction and one unit for multiplication. Produce a table, according to the model below, showing how instructions are executed in consecutive cycles, if we assume in order execution.
c) Rename the registers in the above sequence to prevent, where possible, dependency problems. Produce a second table, according to the model below, showing how instructions (after register renaming) are executed in consecutive cycles, if we assume out of order execution.

In the table cells indicate the sequence number (1, 2, .., 10) of the instruction executed in the corresponding cycle on the respective unit.

	ADD/SUB	ADD/SUB	MUL
Cycle 1			
Cycle 2			
Cycle 3			
. . .			

(4p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

11. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

12. Formulate Amdahl's law and comment.

(3p)

13.
a) What is hardware multithreading?
b) Why do multithreaded processors provide higher performance?
c) We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?

(3p)

14. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)