Försättsblad till skriftlig tentamen vid Linköpings universitet

Datum för tentamen	2015-08-21
Sal (2)	TER3 TERE
Tid	14-18
Kurskod	TDDI03
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Datorarkitektur En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	14
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	013-28 1396
Besöker salen ca klockan	15:30
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Carita Lilja, carita.lilja@liu.se, 1463
Tillåtna hjälpmedel	Ordbok
Övrigt	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2015-08-21, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2015-08-21, kl. 14-18
Du kan skriva på svenska eller engelska!

1.

a) Why do we need special *write strategies* for cache memories?

b). We have discussed three write strategies: *write-through*, *write through with buffered write*, and *copy back*. How do they work? Which are their advantages and disadvantages?

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards. In what consists the particularity and what is the reason behind it?

(2p)

3. Define the three types of pipeline hazards. Give an example for each.

(3p)

4. Branch history table: what does it contain and how is it used?

(2p)

5. Enumerate five of the main characteristics of RISC architectures.

(2p)

6. Dynamic branch prediction with a two-bit scheme. How does it work?
Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        ----------------
LOOP    ----------------
        ----------------
        BNZ     LOOP
        ----------------
```

(3p)

7.

a) What is the role of the page table in a virtual memory system? What data does it store?

b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

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8.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

9.

Consider the following sequence of machine instructions:

```
1:  R1  ←  100
2:  R5  ←  R1 + R2
3:  R7  ←  R5 + 1
4:  R1  ←  R2 * R4
5:  R5  ←  0
6:  R2  ←  R4 - 25
7:  R3  ←  R7 * 2
8:  R4  ←  R1 + R3
9:  R10 ←  0
10: R1  ←  R1 * 30
```

a) Indicate the data dependencies among instructions.

b) Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two units that execute addition&subtraction and one unit for multiplication. Produce a table, according to the model below, showing how instructions are executed in consecutive cycles, if we assume in order execution.

c) Rename the registers in the above sequence to prevent, where possible, dependency problems. Produce a second table, according to the model below, showing how instructions (after register renaming) are executed in consecutive cycles, if we assume out of order execution.

In the table cells indicate the sequence number (1, 2, .., 10) of the instruction executed in the corresponding cycle on the respective unit.

	ADD/SUB	ADD/SUB	MUL
Cycle 1			
Cycle 2			
Cycle 3			
...			

(4p)

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10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

11. What is loop unrolling? How does it work? Why is it important with VLIW architectures? Illustrate by an example.

(3p)

12.
a) What is branch predication (like in the Itanium architecture)?
b) Compare with ordinary branch prediction.

(3p)

13.
a) What is hardware multithreading?
b) Why do multithreaded processors provide higher performance?
c) We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?

(3p)

14. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)