



## Försättsblad till skriftlig tentamen vid Linköpings Universitet

<b>Datum för tentamen</b>	2014-08-22
<b>Sal (1)</b> Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och <u>ringa in</u> vilken sal som avses	TER3
<b>Tid</b>	14-18
<b>Kurskod</b>	TDDI03
<b>Provkod</b>	TEN1
<b>Kursnamn/benämning</b> <b>Provnamn/benämning</b>	Datorarkitektur En skriftlig tentamen
<b>Institution</b>	IDA
<b>Antal uppgifter som ingår i tentamen</b>	14
<b>Jour/Kursansvarig</b> Ange vem som besöker salen	Petru Eles
<b>Telefon under skrivtiden</b>	0703681396
<b>Besöker salen ca kl.</b>	16:00
<b>Kursadministratör/kontaktperson</b> (namn + tfnr + mailaddress)	Carita Lilja, 1463, carita.lilja@liu.se
<b>Tillåtna hjälpmedel</b>	Ordbok
<b>Övrigt</b>	
<b>Vilken typ av papper ska användas, rutigt eller linjerat</b>	
<b>Antal exemplar i påsen</b>	20

LINKÖPINGS TEKNISKA HÖGSKOLA  
Institutionen för datavetenskap  
Petru Eles

**Tentamen i kursen**  
**Datorarkitektur - TDDI03**  
**2014-08-22, kl. 14-18**

**Hjälpmedel:**

Engelsk ordbok.

**Supporting material:**

English dictionary.

**Poänggränser:**

Maximal poäng är 40.  
För godkänt krävs sammanlagt  
21 poäng.

**Points:**

Maximum points: 40.  
In order to pass the exam you need a  
total of minimum 21 points.

**Jourhavande lärare:**

Petru Eles, tel. 0703681396

**Good luck !!!**

Tentamen i kursen Datorarkitektur - TDDI03, 2014-08-22, kl. 14-18

Du kan skriva på svenska eller engelska!

1. Unified caches and separate data and instruction caches: draw a picture for each of the two alternatives and comment on advantages and disadvantages. (3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards. In what consists the particularity and what is the reason behind it? (2p)

3. Define the three types of pipeline hazards. Give an example for each. (3p)

4. Branch history table: what does it contain and how is it used? (2p)

5. Enumerate five of the main characteristics of RISC architectures. (2p)

6. Dynamic branch prediction with a two-bit scheme. How does it work? Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
-----  
LOOP -----  
-----  
BNZ  LOOP  
-----
```

(3p)

7.  
a) What is the role of the page table in a virtual memory system? What data does it store?  
b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

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8.

- a) What is a superscalar architecture?
- b) Draw a block-diagram of a superscalar unit.

(3p)

9.

Consider the following sequence of machine instructions:

- 1.  $R3 \leftarrow R10 + R1$
- 2.  $R7 \leftarrow R5 * 10$
- 3.  $R11 \leftarrow R3 - R0$
- 4.  $R4 \leftarrow R11 - R16$
- 5.  $R10 \leftarrow R7 + 101$
- 6.  $R9 \leftarrow R4 + R12$
- 7.  $R8 \leftarrow R6 * R0$
- 8.  $R2 \leftarrow R4 * R7$
- 9.  $R13 \leftarrow R17 + 2$
- 10.  $R15 \leftarrow R12 * R22$
- 11.  $R14 \leftarrow R15 + 3$

- a) Indicate the data dependencies among instructions.
- b) Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two units that execute addition&subtraction and one unit for multiplication. Produce two tables, according to the model below, showing how instructions are executed in consecutive cycles, if we assume:
  - b1) in order execution
  - b2) out of order execution

In the table cells indicate the sequence number (1, 2, ..., 11) of the instruction executed in the corresponding cycle on the respective unit.

	ADD/SUB	ADD/SUB	MUL
Cycle 1			
Cycle 2			
Cycle 3			
...			

(4p)

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10. Compare VLIW architectures with superscalar architectures:

- a) Show similarities and differences.
- b) Show the advantages and disadvantages of the two approaches.
- c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

11. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

12.

- a) What is branch predication (like in the Itanium architecture)?
- b) Compare with ordinary branch prediction.

(3p)

13.

- a) What is hardware multithreading?
- b) Why do multithreaded processors provide higher performance?
- c) We have described three approaches to multithreading: interleaved, blocked, and simultaneous; what is the main characteristic of each of them?

(3p)

14. What is a vector processor? Draw a block diagram.

What is the basic difference between array processors and vector processors?

(2p)