Försättsblad till skriftlig tentamen vid Linköpings Universitet

Datum för tentamen	2014-04-22
Sal (1) Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och ringa in vilken sal som avses	T1
Tid	14-18
Kurskod	TDDI03
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Datorarkitektur En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	14
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	281396
Besöker salen ca kl.	15:15
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Carita Lilja, 1463, carita.lilja@.liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2014-04-22, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2014-04-22, kl. 14-18
Du kan skriva på svenska eller engelska!

1. Unified caches and separate data and instruction caches: draw a picture for each of the two alternatives and comment on advantages and disadvantages.

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards.
In what consists the particularity and what is the reason behind it?

(3p)

3. Data hazards in pipelines can sometimes be avoided by a technique called *forwarding*. How does this technique work? Give an example in which forwarding produces an acceleration (draw a figure which illustrates the corresponding pipelined execution).

(3p)

4. Branch history table: what does it contain and how is it used?

(2p)

5. Enumerate five of the main characteristics of RISC architectures.

(2p)

6. Dynamic branch prediction with a two-bit scheme. How does it work?
Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        ----------------
LOOP    ----------------
        ----------------
        BNZ     LOOP
        ----------------
```

(3p)

7.

a) What is the role of the page table in a virtual memory system? What data does it store?

b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

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8.

a) What is a superscalar architecture?
b) Draw a block-diagram of a superscalar unit.

(3p)

9.

a) Which are the types of data dependencies that have to be considered with an out-of-order superscalar? Give an example for each.
b) Why do we call them "true" and "artificial", respectively?
c) What can be solved by register renamimg? Give an example.

(3p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why is a superscalar consuming more power, compared to a VLIW computer?

(4p)

11. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

12. What is speculative loading with the Itanium architecture? How does it work?

(3p)

13. Formulate Amdahl's law and comment.

(3p)

14. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)