Försättsblad till skriftlig tentamen vid Linköpings Universitet

Datum för tentamen	2012-04-10
Sal (1) Om tentan går i flera salar ska du bifoga ett försättsblad till varje sal och ringa in vilken sal som avses	TER4
Tid	14-18
Kurskod	TDDI03
Provkod	TEN1
Kursnamn/benämning **Provnamn/benämning**	Datorarkitektur En skriftlig tentamen
Institution	IDA
Antal uppgifter som ingår i tentamen	14
Jour/Kursansvarig Ange vem som besöker salen	Petru Eles
Telefon under skrivtiden	0703681396
Besöker salen ca kl.	15:30
Kursadministratör/kontaktperson (namn + tfnr + mailaddress)	Gunilla Mellheden, 282297, gunilla.mellheden@liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2012-04-10, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2012-04-10, kl. 14-18
Du kan skriva på svenska eller engelska!

1.

a) Why do we need special *write strategies* for cache memories?

b). We have discussed three write strategies: *write-through*, *write through with buffered write*, and *copy back*. How do they work? Which are their advantages and disadvantages?

(3p)

2. Unified caches and separate data and instruction caches: draw a picture for each of the two alternatives and comment on advantages and disadvantages.

(3p)

3. Define the three types of pipeline hazards. Give an example for each.

(3p)

4. Dynamic branch prediction with a two-bit scheme. How does it work?
Illustrate with the case of a loop like the one below. Compare with one-bit prediction.

```
        ----------------
LOOP    ----------------
        ----------------
        BNZ     LOOP
        ----------------
```

(3p)

5. Enumerate five of the main characteristics of RISC architectures.

(3p)

6. The Pentium 4 has a very "extreme" branch prediction technique. What is this technique and what was the motivation for introducing it?

(2p)

7. What is speculative loading with the Itanium architecture? How does it work?

(3p)

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8.

a) Which are the types of data dependencies that have to be considered with an out-of-order superscalar? Give an example for each.

b) Why do we call them "true" and "artificial", respectively?

c) What can be solved by *register renamimg*? Give an example.

(3p)

9. What is the main characteristic of a VLIW processor? What is its main advantage compared to a superscalar?

(3p)

10.

What is loop unrolling? How does it work? Why is it important with VLIW architectures? Illustrate by an example.

(3p)

11. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

12. What is the role of the mask register in a vector unit? Give an example.

(3p)

13.

a) What is the basic idea with the MMX extensions to the INTEL architecture?

b) Give an example with packing and one with unpacking of MMX data.

(3p)

14. What is hardware multithreading?
Why do multithreaded processors provide higher performance?

(2p)