Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	101216
Sal	KÅRA
Tid	8-12
Kurskod	TDDI03
Provkod	
Kursnamn/benämning	Datorarkitektur
Institution	*IDA*
Antal uppgifter som ingår i tentamen	14
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	0703681396
Besöker salen ca kl.	10
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, 282297, gunilla.mellheden@liu.se
Tillåtna hjälpmedel	Engelk ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2010-12-16, kl. 8-12

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2010-12-16, kl. 8-12
Du kan skriva på svenska eller engelska!

1. Unified caches and separate data and instruction caches: draw a picture for each of the two alternatives and comment on advantages and disadvantages.

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards.
In what consists the particularity and what is the reason behind it?

(3p)

3. Comment on the evolution of the pipeline organization from ARM7 to ARM9 and ARM11 and how the performance increase has been obtained.

(3p)

4. Data hazards in pipelines can sometimes be avoided by a technique called *forwarding*. How does this technique work? Give an example in which forwarding produces an acceleration (draw a figure which illustrates the corresponding pipelined execution).

(3p)

5. Delayed load. Why do we need it with RISC architectures? How does it work?
Give an example.

(3p)

6.

a) What is the role of the page table in a virtual memory system?

b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

7.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

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8. Give an example with o*utput dependency* and another one with *antidependency.* Show how they can be solved by *register renamimg*.

(3p)

9. Enumerate five of the main characteristics of RISC architectures.

(2p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why ia a superscalar consuming more power, compared to a VLIW computer?

(3p)

11. What is speculative loading with the Itanium architecture? How does it work?

(3p)

12. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

13. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)

14. What is hardware multithreading?
Why do multithreaded processors provide higher performance?

(3p)