Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2010-08-21
Sal	TER3
Tid	14-18
Kurskod	TDDI03
Provkod	
Kursnamn/benämning	Datorarkitektur
Institution	*IDA*
Antal uppgifter som ingår i tentamen	14
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Soheil Samii
Telefon under skrivtid	0707482651
Besöker salen ca kl.	16
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, 282297, gunilla.mellheden@liu.se
Tillåtna hjälpmedel	Ordbok
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2010-08-21, kl. 14-18

Hjälpmedel:

Engelsk ordbok.

Supporting material:

English dictionary.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Soheil Samii, tel. 0707482651

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2010-08-21, kl. 14-18
Du kan skriva på svenska eller engelska!

1. Unified caches and separate data and instruction caches: draw a picture for each of the two alternatives and comment on advantages and disadvantages.

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards.
In what consists the particularity and what is the reason behind it?

(3p)

3. Define the three types of pipeline hazards. Give an example for each.

(3p)

4. Branch history table: what does it contain and how is it used?

(2p)

5. Delayed load. Why do we need it with RISC architectures? How does it work?
Give an example.

(3p)

6.

a) What is the role of the page table in a virtual memory system?

b) The page table is very large, usually too large to be stored in main memory. Such a large size, at the same time, makes access to the page table very slow. How is this solved in current microprocessor architectures.

(3p)

7.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

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8. Give an example with o*utput dependency* and another one with *antidependency.* Show how they can be solved by *register renamimg*.

(3p)

9. The design of RISC architectures is based on certain characteristics of typical programs which are frequently used. Enumerate at least five such characteristics of programs.

(2p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why ia a superscalar consuming more power, compared to a VLIW computer?

(4p)

11.
a) What is branch predication (like in the Itanium architecture)?
b) Compare with ordinary branch prediction.

(3p)

12.
a) What is the basic idea with the MMX extensions to the INTEL architecture?
b) Give an example with packing and one with unpacking of MMX data.

(3p)

13. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(2p)

14. What is the role of the mask register in a vector unit? Give an example.

(3p)