Försättsblad till skriftlig tentamen vid Linköpings universitet

(fylls i av ansvarig)

Datum för tentamen	2009-12-15
Sal	T1&T2
Tid	8-12
Kurskod	TDDI03
Provkod	
Kursnamn/benämning	Datorarkitektur
Institution	*IDA*
Antal uppgifter som ingår i tentamen	14
Antal sidor på tentamen (inkl. försättsbladet)	4
Jour/Kursansvarig	Petru Eles
Telefon under skrivtid	0703681396
Besöker salen ca kl.	10
Kursadministratör (namn + tfnnr + mailadress)	Gunilla Mellheden, gunme@ida.liu.se, 2297
Tillåtna hjälpmedel	Ordbuk
Övrigt (exempel när resultat kan ses på webben, betygsgränser, visning, övriga salar tentan går i m.m.)	
Vilken typ av papper ska användas, rutigt eller linjerat	
Antal exemplar i påsen	

LINKÖPINGS TEKNISKA HÖGSKOLA
Institutionen för datavetenskap
Petru Eles

Tentamen i kursen

Datorarkitektur - TDDI03

2009-08-18, kl. 8-12

Hjälpmedel:

Inga.

Supporting material:

No supporting material allowed.

Poänggränser:

Maximal poäng är 40.
För godkänt krävs sammanlagt 21 poäng.

Points:

Maximum points: 40.
In order to pass the exam you need a total of minimum 21 points.

Jourhavande lärare:

Petru Eles, tel. 0703681396

Good luck !!!

Tentamen i kursen Datorarkitektur - TDDI03, 2009-12-15, kl. 8-12
Du kan skriva på svenska eller engelska!

1.

a) Why do we need special *write strategies* for cache memories?

b). We have discussed three write strategies: *write-through*, *write through with buffered write*, and *copy back*. How do they work? Which are their advantages and disadvantages?

(3p)

2. The Pentium 4 has an L1 instruction cache which is particular in several regards. In what consists the particularity and what is the reason behind it?

(3p)

3. Define the three types of pipeline hazards. Give an example for each.

(3p)

4. Comment on the evolution of the pipeline organization from ARM7 to ARM9 and ARM11 and how the performance increase has been obtained.

(3p)

5. Branch history table: what does it contain and how is it used?

(2p)

6. The Pentium 4 has a very "extreme" branch prediction technique. What is this technique and what was the motivation for introducing it?

(2p)

7.

a) What is a superscalar architecture?

b) Draw a block-diagram of a superscalar unit.

(3p)

8. Give an example with o*utput dependency* and another one with *antidependency*. Show how they can be solved by *register renamimg*.

(3p)

Tentamen i kursen Datorarkitektur - TDDI03, 2009-12-15, kl. 8-12
Du kan skriva på svenska eller engelska!

9. The design of RISC architectures is based on certain characteristics of typical programs which are frequently used. Enumerate at least five such characteristics of programs.

(2p)

10. Compare VLIW architectures with superscalar architectures:
a) Show similarities and differences.
b) Show the advantages and disadvantages of the two approaches.
c) Why ia a superscalar consuming more power, compared to a VLIW computer?

(4p)

11.
a) What is branch predication (like in the Itanium architecture)?
b) Compare with ordinary branch prediction.

(3p)

12.
a) What is the basic idea with the MMX extensions to the INTEL architecture?
b) Give an example with packing and one with unpacking of MMX data.

(3p)

13. What is a vector processor? Draw a block diagram.
What is the basic difference between array processors and vector processors?

(3p)

14. Formulate Amdahl's law and comment.

(3p)