Exam, Mixed-Signal System Design (DAT116)

January 16, 2016

Time and place: Saturday January 16, 8:30 – 12:30, Hörsalslängan

Examiner: Lars Svensson, Lena Peterson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (extension 1704); will visit the room at 9:30 and at 11:30

Solutions: Will be posted on the course homepage on January 20

Results: Will be posted in LADOK on or before February 3

Grading review: Time and place to be posted on the course homepage

Grade limits:

U: 0–29 points; 3: 30–39 points; 4: 40–49 points; 5: 50– points

Bonus points from omnibus report will be added to the score before computing the final grade.

Allowable references and utilities: Open-book exam. Text books, lecture notes, research article printouts, and lab reports are admissible. Errata sheet printout for textbooks are also OK, as is a calculator.

General: Submit your solutions, ***in English***, on blank papers sheets. Write legibly; feel free to use figures to get your point across.

Please start the solution for each problem on a new sheet. Please number the sheets so that solutions are in numerical order.

In some problems, it may be necessary to make assumptions or to introduce variables etc. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions may give partial credit even if the end result is not 100% correct.

Please note that your personal identity code is required on each submitted sheet!

Good luck!

Problems

Each sub-problem is worth five points, for a total of 60 points.

You may need the value of Bolzmann's constant: $k = 1.38 \times 10^{-23}$ J/K. These trigonometrical identities may also come in handy:

$$\sin 2\alpha = 2 \sin \alpha \cos \alpha$$

$$\cos 2\alpha = \cos^2 \alpha - \sin^2 \alpha$$

$$\sin 3\alpha = 3 \sin \alpha - 4 \sin^3 \alpha$$

$$\cos 3\alpha = 4 \cos^3 \alpha - 3 \cos \alpha$$

$$\sin 4\alpha = 4 \sin \alpha \cos \alpha - 8 \sin^3 \alpha \cos \alpha$$

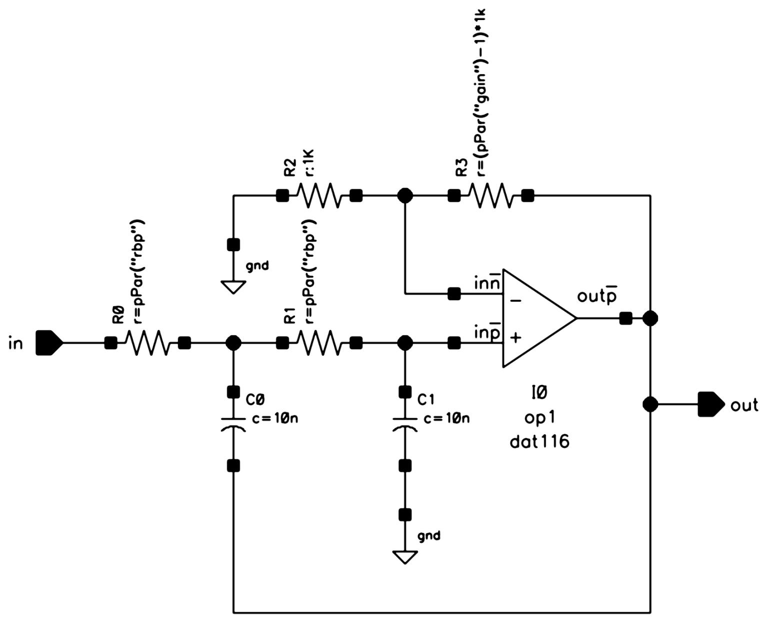
$$\cos 4\alpha = 8 \cos^4 \alpha - 8 \cos^2 \alpha + 1$$

1. In a DAT116 lecture, Emilia learns about the pipelined AD converter with one-bit stages. She immediately realizes that it would be possible to use only *one* hardware stage, and re-circulate the signal through that stage until the desired (and easily configurable!) number of bits have been extracted[1]. To evaluate her idea, she assumes a signal frequency of 10 MHz and a maximum clock frequency of 300 MHz.
   (a) Estimate the maximum SNDR that might be reached if one bit decision can be made per clock cycle.
   (b) Calculate the sample-clock jitter requirement for the maximum-SNDR configuration of the previous subtask.
   (c) Discuss the matching requirements of the passive components in the hardware stage. How do these requirements depend on the resolution used?
   (d) Assume a switched-capacitor implementation with component matching according to the previous task. How will the minimum power dissipation scale with the resolution used?

2. A noise-shaping first-order sigma-delta loop is used for digital-to-analog conversion. The sigma-delta loop generates a signal of higher sample rate but lower resolution than the original digital signal; the new signal is then fed into a low-resolution DAC. The required signal bandwidth for the system is 15 MHz; the final DAC has a maximum conversion rate of 900 million conversions per second. The overall SNDR requirements for the system is specified as 53 dB at an output power 2 dB below the full-scale signal.
   (a) Estimate the DAC resolution necessary to fulfill the SNDR requirement.
   (b) In an attempt to reduce power dissipation, Emil considers replacing the first-order loop with a second-order loop. Estimate the factor by which the conversion rate may be reduced if the DAC resolution, signal bandwidth, and overall SNR requirement are unchanged.
   (c) The output DAC is built from a thermometer-coded row of current sources. A manufacturing gradient causes a linear increase in the current values along the row of sources. For the first-order loop, how small must the ratio of the first-source and last-source current be for the associated error to be smaller than the errors considered in task 2a above?

[1] As she will learn later, this is not an original insight.

3. In Lab 4, you studied a time-continuous filter implemented with two instances of a second-order section. The figure below shows the circuit schematic of the Lab-4 filter section; the table lists nominal parameters for the highest-Q instance.

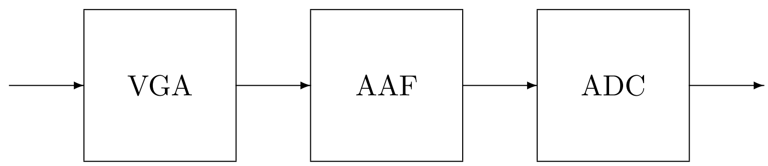


R0, R1	3.30k
DC gain (A)	2.78
Q	$1/(3-A) \approx 4.55$

(a) First, assume that the circuit op-amp is ideal. Estimate the necessary matching accuracy for R_2 and R_3 to limit the overall filter-specification violation to at most 0.5 dB.

(b) Next, replace the ideal op-amp with a somewhat more realistic version, with a single dominant pole and a gain-bandwidth product of 3 MHz. Re-estimate the matching requirement for this case.

4. A certain mixed-signal system is used to record a narrow-band signal generated by a novel biomedical sensor. The signal in question can be viewed as a sum of two sine waves with the same power but slightly different angular frequencies (ω_1 and ω_2). In order to best use the ADC range, the system includes a variable-gain amplifier (VGA) before the anti-aliasing filter (as illustrated below), and an automatic gain control (AGC) mechanism to adjust the signal level at the input of the ADC to cover the full ADC range.



   (a) What is the power of each of the two sine waves at the input of the ADC, relative to the power of a single full-scale sinewave?

   (b) The VGA suffers from a symmetrical third-order nonlinearity, such that the instantaneous value of the output signal y for an input signal x is given by:

   $$y(t) = G \cdot (x(t) - \alpha \cdot (x(t))^3)$$

   where G is the amplifier gain, and the parameter α determines the severity of the nonlinearity. Derive the SNDR at the output of the VGA as a function of α, disregarding any DC error and assuming that the anti-aliasing filter will remove any intermodulation products far away from ω_1 and ω_2. You may assume that α takes small positive values.

   (c) Suggest a suitable resolution for the quantizer of this system. *Motivate your suggestion.*

THE END