Exam, Mixed-Signal System Design (DAT116)

Jan 17, 2015

Time and place: Saturday Jan 17, 8:30 – 12:30, V building

Examiner: Lars Svensson, Lena Peterson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (extension 1704); will visit the room at 9:30 and at 11:30

Solutions: Will be posted on the course homepage on Jan 19

Results: Will be posted in LADOK on or before Feb 4, 2015

Grading review: Feb 6, 2015; time and place to be posted on the course homepage

Grade limits:

U: 0-29 points; 3: 30-39 points; 4: 40-49 points; 5: 50- points

Bonus points from omnibus report will be added to the score before computing the final grade.

- Allowable references and utilities: Open-book exam. Text books, lecture notes, research article printouts, and lab reports are admissible. Errata sheet printout for textbooks are also OK, as is a calculator.
- **General:** Submit your solutions, *in English*, on blank papers sheets. Write legibly; feel free to use figures to get your point across.

Please start the solution for each problem on a new sheet. Please number the sheets so that solutions are in numerical order.

In some problems, it may be necessary to make assumptions or to introduce variables etc. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions may give partial credit even if the end result is not 100% correct.

Please note that your personal identity code is required on each submitted sheet!

Good luck!

Problems

Each sub-problem is worth five points, for a total of 60 points. Figures are collected at the back of the pack.

- 1. A low-pass signal with a bandwidth of 7 MHz is to be sampled and converted to digital form. The overall peak-SNR requirement is 48 dB.
 - (a) Suggest minimum values of clock frequency and quantizer resolution to fulfill the specifications.
 - (b) Suggest a maximum clock jitter value which will allow the specifications to be fulfilled together with the limited resolution from the previous subtask.
 - (c) Outside the band of interest, uninteresting and potentially destructive signals (i.e. noise) can occur at the same power levels as those in the band of interest. How will you select the sample rate if you can afford a pre-sampling anti-alias filter of at most order 3? Motivate.
- 2. A certain signal conditioning chain includes a programmable gain amplifier (PGA) which is to amplify the signal by 0, 20, or 40 dB. The band of interest is from 50 Hz to 1 kHz; the gain error must be at most 1% across the band for all gain settings.

Two proposed designs are based on the amplifier OP27 with resistive feedback in a non-inverting configuration as in Figure 1. The OP27 open-loop gain curve can be found in Figure 2.

The first proposed design consists of one stage with three alternate values of R2 which will be switched in to provide the three gain levels. The second design consists of two identical stages, each with two choices of R2 for 0 and 20 dB.

- (a) Which of the two solutions is preferrable? Motivate!
- (b) Estimate the resistor matching precision needed to reach the gain error of 1% across the band for the case you preferred in task 2a.
- (c) A similar on-chip PGA is based on an op-amp with a gain-bandwidth product of 20 MHz. Estimate the ratio of the total resistor areas needed for the one-stage and the two-stage solutions. Assume the same gain settings and gain error as in the OP27 case, and that the same R1 value will be used in both designs.

[This problem was inspired by the MSc project of EESD student Mahmoud Tour.]

- 3. (a) A 10-bit A/D converter uses time-interleaving with two signal branches. At what level of inter-path gain error does this error contribute as much to the SNDR as does the quantization noise?
 - (b) In the same converter as in the previous task, what level of sample time skew will cause an error of equal magnitude?
 - (c) In a *three*-path time-interleaved converter, what will be the frequences of spurious signals caused by gain errors?

- 4. Figure 3 shows a proposed method to design a hybrid digital/analog reconstruction filter for an oversampled, one-bit D-to-A converter¹. The data sequence bits are used to select whether to inject each current term into the virtual-ground node of the output integrator. The currents a_i provide the values for the discrete-time low-pass filter impulse response.
 - (a) Estimate the possible peak SNDR of the DAC under the "perfect-lowpass-filter" assumption used during the course. Assume an OSR of 64 and a second-order loop filter.
 - (b) As mentioned above, the sequence of current terms constitute the discrete-time impulse response of the reconstruction filter. A simple (albeit far from optimal) case is when all currents are designed to be equal; the rectangular impulse response corresponds to a weak low-pass characteristic ($\sin x \equiv (\sin \pi x)/\pi x$), as illustrated in figure 4. Suggest a suitable impulse-response length and estimate the noise suppression possible with such a filter! (A coarse estimate is better than no estimate; better estimates get more points.)
 - (c) The current-to-voltage conversion in the output buffer adds an extra pole to the reconstructionfilter response. Assume that the converter is to be used for audio signals and suggest how to select the values of the passive components.

THE END

¹See D. Su and B. Wooley: A CMOS oversampling D/A converter with a current-mode semidigital reconstruction filter. IEEE Journal of Solid-State Circuits, December 1993. [The claimed benefits include lower system cost (as any additional off-chip filter may be very simple), and higher linearity than for a "traditional" current-summing D-to-A converter (since a current-source mismatch will affect the filter impulse response rather than the converter DNL).]



Figure 1: Non-inverting amplifier configuration.



Figure 2: OP27 open-loop gain curve.



Figure 3: Semidigital FIR filter: block diagram (a) and rough schematic (b).



Figure 4: A sinc magnitude function corresponding to a rectangular impulse response of length T.